

RESEARCH

(Krishnaiyan Thulasiraman)

Research has been organized into twelve sections under the following categories:

- Network Analytics/Science and Engineering
- Fault Tolerance in Networks and Systems
- Traffic Engineering: Routing, Protocol Testing and Topology Abstraction Service
- Marked Graphs and Parallel and Distributed Computations on Graphs and Networks
- VLSI
- Graph Theory

NETWORK ANALYTICS/ SCIENCE AND ENGINEERING

I. Algebraic Theory of Resistive Networks: Bridging Electrical Circuit Theory and Modern Advances in Network Science/Engineering

A resistive network is a weighted graph in which each edge is a resistance element with its weight equal to its resistance or conductance value. A multiport resistive network is characterized by the relationships between the voltages and currents as seen across the pairs of terminals of the network called ports. Two common characterizations n-port networks are the short-circuit conductance matrix Y and the open-circuit resistance matrix Z that relate the port current vector I and the port voltage vector V as $I= YV$ and $V=ZI$, respectively. Given Y or Z the multiport resistive network synthesis problem is to design a resistive network which has Y or Z as its characterizing matrix. This problem received considerable attention in the circuit theory literature in the 1960's and 1970's because this was considered as the first step towards the design of general multiport networks that contain inductances and capacitances in addition to resistances. A significant body of knowledge on this problem is now available in the literature. Though both resistive network theory and network flow theory were both developed in parallel by two research communities (Electrical Engineering and Operations Research) there was not much interest in resistive networks beyond 1980 because of the lack of immediate applications. There was a dramatic turn of events when about a decade ago Professor Doyle at Caltech wrote a book connecting random walks in communication networks and current flows in resistive networks. This modelling power of resistive networks triggered a renewed interest in this area because of its applications in communication networks, social networks and power networks.

As outlined later below, the foundation of most of the modern applications of resistive network theory may be found in the results developed by Professor Thulasiraman and his team during 1965-1980.

In the multiport network synthesis area there were two directions of research... networks in which the ports form a connected structure (a tree) and those in which the port structure is not connected. When Professor Thulasiraman started his research career in 1965, the synthesis problem was settled with ground-breaking contributions by legendary circuits and systems theorists, to name a few, Professors Guillemin (MIT), Israel Cederbaum (Teknion), Masao Iri (Univ. Of Tokyo), Robert Newcomb (Maryland), Frank Boesch (Bell Labs.), Biorci and Civalleri (Italy) etc. The difficult problem of synthesis when the port structure is not connected remained largely unexplored and provided Professor Thulasiraman rich opportunities for contributions. Professor KT's first result was a comment [1.1] in which he pointed out a flaw in Cederbaum's network equivalence theory and provided a remedy to fix this flaw. This led him and his team of students and co-workers to publish a series of papers culminating in a theory and algorithmic framework for the multiport resistive network synthesis problem.

Professor KT's major contributions are:[1.1] – [1.28] introduction of the concepts of modified cutset matrix and modified circuit matrix ; introduction of the concept of the potential factor matrix ; an equivalence theory based on these matrices; a general theoretical framework for the multiport resistive network synthesis problem; introduction of the concepts of parallel and pseudo series combinations formalizing these ideas presented earlier by Guillemin;

synthesis procedures for several classes of Y matrices and generation of equivalent n -port networks; synthesis of networks having specified sensitivity coefficients based on Director and Rohrer's adjoint technique for sensitivity computation.

As pointed below, all these contributions have significant impact on advances in the modern area of network science/engineering.

1.1 Congestion control under random walk routing in communication networks

Routing is the most fundamental aspect of communication and transportation networks. Given a weighted network, a random walk routing starts at a node and follows links determined by a probabilistic measure based on the weights of the links incident at each node encountered in the walk. It has been shown by Doyle and others that the congestion (total number of links traversed) by a random walk from a node a to a node b is proportional to the resistance distance (same as input resistance) between these nodes in a resistance network which has the same topology as the given communication network and the weights of the links are the same as the conductance's of the links. The congestion control problem is to determine the link weights (conductances) that achieve a desired level of congestion under a random walk routing between two nodes. The equivalence theory and formulations developed in [1.10] which is considered as a pioneering work (see the Appendix on Awards and Recognitions) contain all the information needed to design link weights to achieve the required level of congestion in a random walk routing. This is a remarkable result which would not have been possible but for the works of Professor KT.

1.2 Flow Preserving Power Equivalents for Market Analysis

Modern power systems are very large electrical networks. Analysis of such networks is computationally very expensive. To mitigate the complexity of analyzing these networks, simpler networks preserving certain properties of the original network is desired. In power market analysis simpler equivalent networks in which power flows along a given set of transmission lines are the same as those in the original network under a given set of operating conditions. Recently Professor Thulasiraman has developed a theory to determine such equivalents which generalizes the currently available approaches. In a preliminary version of this work he introduced [1.29] the concept of average electrical distance between a bus and a transmission line, and combined it with a clustering procedure to determine a flow preserving equivalent network. In subsequent works under preparation he has developed a generalized theory of flow preserving equivalents that are also robust to varying operating conditions.

1.3 Vulnerability Assessment of Power Grids against Cascading Failures

In [1.30] Professor KT has shown how the concept of resistance distance can be used to develop what are called the betweenness measures of links and nodes for vulnerability assessment of large power networks against cascading failures. Note that betweenness measures of links and nodes are concepts introduced in the context of social network analysis and refer to their importance in the broadcast of information between nodes.

1.4 Algebraic Graph Theory, Electrical Circuit Theory and Social Network analysis

Algebraic graph theory refers to the study of structural properties of graphs using linear algebraic concepts such as circuit, cutset, Laplacian and adjacency matrices of a graph and their determinants, cofactors and eigenvalues. In social network analysis, the concept of Laplacian matrix plays a central role. Interestingly, the Laplacian matrix is the same as the Y matrix (also same as the node to datum conductance matrix of a multi-port resistance network). Also, the concept of Kirchhoff index introduced by the molecular chemistry community is relevant for social network analysis because it is the sum of resistance distances between all pairs of nodes in a graph and captures the impact of all paths between pairs of nodes. In view of these connections, all the results on resistance networks developed by Professor KT and discussed in this section are relevant to social network analysis.

In [1.31] Professor KT has discussed a number of new results generalizing the concept of the Laplacian matrix and how these results could be used to develop formulas for Kirchhoff Index. Professor KT has also discussed in this paper various applications of his works for social network analysis such as the problem of detecting of the presence

of communities in social networks. and how these problems can be solved using his findings in [1.10]. Applications of Kirchhoff Index in communication networks are given in [1.32] and [1.33].

In 1949 and 1962 Ronald M. Foster, the legendary circuit theorist, presented two theorems which contain invariants involving resistance distances between all pairs of nodes of a graph. After about five decades these results have been found useful by the computer science community for the computational complexity analysis of online algorithms. Several mathematicians have attempted to find a generalized version of Foster's theorems, but failed. In [1.31] Professor KT has given a generalization using the concept of Kroon's reduction. In an earlier work [1.34] he gave a graph theoretic proof of Foster's original theorem.

1.5 Sensitivity Invariants for Linear and Nonlinear Circuits: Similar to Foster's results on network invariants, Professor KT presented in [1.35- 1.39] several invariant results for linear and nonlinear electrical circuits. These results are purely graph theoretic and are based on Tellegen's theorem.

The applications of resistance network theory discussed above are all with respect to network science/engineering. There are several other areas (outside of electrical engineering) such as biostatistics and combinatorial designs in coding theory where these results are found useful.

References:

- [1.1] S. Srinivasan, V. N. Sujeer and K. Thulasiraman, "[Application of Equivalence Technique in Linear Graph Theory to Restoration Process in a Power System](#)", *Journal of the Institution of Engineers, (India), Vol. XLVII, No. 10, June 1967, pp. 526-543.*
- [1.2] S. Srinivasan, V. N. Sujeer and K. Thulasiraman, "[Application of Equivalence Technique in Linear Graph Theory to Reduction Process in a Power System](#)", *Journal of the Institution of Engineers, (India), vol. XLVI, No. 12 June 1966, pp. 528-549.*
- [1.3] K. Thulasiraman and V. G. K. Marti, "[Comments on 'On Equivalence of Resistive n-Port Networks'](#)", *IEEE Trans. on Circuit Theory, Vol. CT-14, September 1967, pp. 357-359.*
- [1.4] V. G. K. Marti and K. Thulasiraman, "[Synthesis of a Class n-port Networks](#)", *IEEE Trans. on Circuit Theory, Vol. CT-15, March 1968, pp. 54-64.*
- [1.5] K. Thulasiraman and V. G. K. Marti, "[Pseudo-Series Combination of n-port Networks](#)", *Proc. IEEE, Vol. 56, June 1968, pp. 1143-1144.*
- [1.6] K. Thulasiraman and V. G. K. Marti, "[Parallel Connection of n-port Networks](#)", *Proc. IEEE, Vol. 55, July 1967, pp. 1216-1217.*
- [1.7] K. Thulasiraman and V. G. K. Marti, "[Synthesis Application of the Modified Cutest Matrix](#)", *Proc. IEE, London, Vol. 115, Sept. 1968, pp. 1269-1274.*
- [1.8] K. Thulasiraman and V. G. K. Marti, "[The Modified Cutest Matrix of an n-port Network](#)", *Proc. IEE London, Vol. 115, Sept. 1968, pp. 1263-1268.*
- [1.9] C. Eswaran and K. Thulasiraman, "[Synthesis of a Class of Resistive 3-port Networks](#)", *International Journal of Electronics, 1968 Vol 24 pp. 597-603.*
- [1.10] K. Thulasiraman and V. G. K. Marti, "[The Modified Circuit Matrix of an n-port Network and its Applications](#)", *IEEE Trans. on Circuit Theory, Vol. CT-16, February 1969, pp. 2-7.* Also presented at the 1968 First International Symposium on Circuit Theory.
- [1.11] P. S. Reddy and K. Thulasiraman, "Synthesis of the K-matrix of an N-port Network and its Application to Y-matrix Synthesis", *Proc. IEEE Intl. Symp. on Circuit Theory, 1970.*

- [1.12] P. S. Reddy and K. Thulasiraman, "Synthesis of K-Matrix of (n+1)-node Resistive n-port Networks", Proc. Asilomar Conference on Circuits and Systems, November pp. 588- 590, 1971.
- [1.13] M. N. S. Swamy and K. Thulasiraman, "Synthesis of Multivariable Networks", Proc. Asilomar Conference on Circuits and Systems, November 1971, pp. 571-575.
- [1.14] M. N. S. Swamy, and K. Thulasiraman, "*Realization of the A-Matrix of RLC Networks*", IEEE Trans. on Circuit Theory, Vol. CT-19, Sept. 1972, pp. 515-518.
- [1.15] M. N. S. Swamy, and K. Thulasiraman, "*A Sufficient Condition for the Synthesis of the K-Matrix of n-Port Networks*", IEEE Trans. on Circuit Theory, Vol. CT-19, July 1972, pp. 378-380.
- [1.16] P. S. Reddy and K. Thulasiraman, "*Synthesis of (n+2)-node Resistive n-Port Networks*", IEEE Trans. on Circuit Theory, Vol. CT-19, January 1972, pp. 20-25.
- [1.17] P. A. Ramamoorthy, K. Sankar Rao and K. Thulasiraman, "Synthesis of Rational Voltage Transfer Matrices Using Minimum Number of Capacitors with Operational Amplifiers", Proc. IEEE International Symposium on Circuit Theory, April 1973, pp. 294-297.
- [1.18] P. A. Ramamoorthy and K. Thulasiraman, "*Active RC n-port Network Synthesis Using Nullators and Norators*", IEEE Trans. on Circuit Theory, Vol. CAS-21, March 1974, pp. 206-209. August 1977.
- [1.19] M. G. G. Naidu, P. S. Reddy and K. Thulasiraman, "*Synthesis of Resistive Networks from Third Order Paramount Matrices*", IEEE Trans. on Circuits and Systems, Vol. CAS-22, Dec. 1975, pp. 937-943.
- [1.20] M. G. G. Naidu, K. Thulasiraman and M. N. S. Swamy, "*The n-port Resistive Network Synthesis from Prescribed Sensitivity Coefficients*", IEEE Trans. On Circuits and Systems, Vol. CAS-22, June 1975, pp. 482-485.
- [1.21] P. S. Reddy and K. Thulasiraman, "*Analysis and Synthesis of the K and Y Matrices of Resistive n-port Networks*", Z. Elektr. Inform. U. Energietechnik, Leipzig 5, 1975, pp. 81-96.
- [1.22] M. G. G. Naidu, P. S. Reddy and K. Thulasiraman, "*(n+2)-node Resistive n-port Realizability of Y-Matrices*", IEEE Trans. on Circuits and Systems, Vol. CAS-23, May 1976, pp. 254- 261.
- [1.23] P. S. Reddy and K. Thulasiraman, "*Synthesis of the K-Matrix of (N+3)-node Resistive n-port Networks*", Z. Elektr. Inform. U. Energietechn
- [1.23] M. G. G. Naidu, P. S. Reddy and K. Thulasiraman, "*Continuously Equivalent Realizations of 3rd-order Paramount Matrices*", International Journal of Circuit Theory and Applications, Vol. 5, 1977, pp. 403-408.
- [1.25] M. G. G. Naidu, P. S. Reddy and K. Thulasiraman, "*On the Number of Conductances Required for Realizing Y and K Matrices*", International Journal of Circuit Theory and Applications, Vol. 5, 1977, pp. 219-225.
- [1.26] P. A. Ramamoorthy and K. Thulasiraman, "*Active RC n-port Network Synthesis Using Nullators and Norators*", IEEE Trans. on Circuit Theory, Vol. CAS-21, March 1974, pp. 206-209. August 1977.
- [1.27] K. Thulasiraman, M. N. S. Swamy and P. S. Reddy, "*(N+P)-node Realizability of Y-Matrices of (N+1)-node Resistance Networks*", International Journal of Circuit Theory and Applications, Vol. 6, 1978, pp. 253-263.
- [1.28] K. Thulasiraman, "*On Description and Realization of Resistance n-port Networks*", IEEE Trans. on Circuits and Systems, Vol. CAS-32, March 1985, pp. 296-297.
- [1.29] Dhruv Sharma, Krishnaiyan Thulasiraman, Di Wu and John N. Jiang, "A Network Science Based K-Means +++ Clustering Method for Power Network Equivalencing ", *Computational Social Networks*, , 6:4 , 2019, Springer Nature , <http://doi.org/10.1186/s40649-019-0064-3>

- [1.30] Di Wu, Feng Ma, Milad Javadi, Krishnaiya Thulasiraman, Ettore Bompard, John N. Jiang, “A study of the impacts of flow direction and electrical constraints on vulnerability assessment of power grid using electrical betweenness measures” *Physica A* 466 (2017), Elsevier Publishing Company pp 295-309.
- [1.31] Krishnaiyan Thulasiraman, Mamta Yadav and Kshirasagar Naik, “Network Science meets Circuit Theory: Resistance Distance, Kirchhoff Index/Network Criticality and Foster’s Theorems with Unification and Generalization”, *IEEE Transactions on Circuits and Systems*. Vol. 66,NO.3, March 21019
- [1.32] Ziping Hu, Krishnaiyan Thulasiraman and Pramode K. Verma, “Complex Networks: Traffic Dynamics, Network Performance, and Network Structure,” *American Journal of Operations Research*, Vol.3, 2013, 187-195.
- [1.33] Ziping Hu, Pramode K. Verma and K. Thulasiraman, “Local flow distribution and optimal weighting against congestion and cascading failures in weighted complex networks” *ECCS* 13.
- [1.34] K. Thulasiraman, R. Jayakumar and M. N. S. Swamy, “[Graph Theoretic Proof of a Network Theorem and Some Consequences](#)”, *Proc. IEEE*, June 1983, pp. 771-772.
- [1.35] M. N. S. Swamy, C. Bhushan and K. Thulasiraman, “[Sensitivity Invariants for Linear Time- invariant Networks](#)”, *IEEE Trans. on Circuit Theory*, Vol. CT-20, January 1973, pp. 21-24.
- [1.36] M. N. S. Swamy, C. Bhushan and K. Thulasiraman, “Sensitivity”, *IEEE Trans. on Circuit Theory*, Vol. CT-19, November 1972, pp. 599-606..
- [1.37] M. N. S. Swamy, C. Bhushan and K. Thulasiraman, “Sensitivity”, *Electronics Letters*, January 1972, pp. 26-27. See also *ISCAS* 1972
- [1.38] M. N. S. Swamy, C. Bhushan and K. Thulasiraman, “[Simple Sensitivity Formulas in Terms of Immittance Parameters](#)”, *Electronics Letters*, March 1972, pp. 153-154.
- [1.39] M. N. S. Swamy, C. Bhushan and K. Thulasiraman, “[Bounds on the Sum of Element Sensitivity Magnitudes for Network Functions](#)”, *IEEE Trans. on Circuit Theory*, Vol. CT-19, Sept. 1972, pp. 502-504

FAULT TOLERANCE IN NETWORKS AND SYSTEMS

Rapid advances in semiconductor technology have led to the fabrication of large scale circuits and systems whose components are prone to failures. This motivated the study of fault tolerance of networks and systems. Most of the research in this area has focused on the impact of the topology on the fault tolerance of networks and systems. Research in this area has focused on the following issues:

- Testing if a system is faulty.
- Diagnosis/location of faulty components.
- Diagnosability (ability) of a system to be diagnosed under a given fault model.

Professor KT has made extensive contributions to all the above aspects in a variety of applications as discussed below.

II. System level Diagnosis: Diagnosis and Diagnosability of Multiprocessor Systems

The area of system level diagnosis was pioneered by Preparata, Metze and Chien (PMC) of the University of Illinois in early 1960s. Given a multi-processor system in which some of the processors could be faulty. To diagnose/locate the faulty processors, each processor is allowed to test a subset of the processors. Note that the subset of processors tested by a processor is yet to be determined. If a processor i tests a processor j and finds it is faulty then the test

outcome is designated as 1; otherwise the test outcome is 0. Note that the test outcome of a faulty processor is not reliable. In other words, a faulty processor may test a faulty processor as fault-free. Each test by a processor i on a processor j is denoted by a link (i, j) directed from i to j . The collection of all test links forms the test graph (also called the system graph) which is a directed graph. The model presented above is called the PMC model.

A system is t -diagnosable under the PMC model if all the faulty processors can be uniquely diagnosed if there are at most t faulty processors in the system. The following questions arise:

- Given t , determine if a system is t -diagnosable.
- Diagnose all the faulty processors in a t -diagnosable system.
- Determine the maximum value of t for which a system is t -diagnosable. This number is called the diagnosability of the system.

Professor KT has made a number of pioneering contributions to the above problems and similar problems for fault models other than PMC model.

Unique diagnosis requirement imposed by a t -diagnosable system imposes severe constraints on its connectivity and so requires a large number of tests. To address this problem the concept of t/s -diagnosable system was introduced. A system is t/s -diagnosable if it is possible to locate a subset of s processors which include all faulty processors, assuming that there are at most t faulty processors. Professor KT has made two breakthrough contributions to theory of t/s diagnosable systems. These results extend those given earlier by Hakimi, Amin, Chwa, Dahburra and Mason for t -diagnosable systems. In [2.1] he provided an algorithm for t/s diagnosis which is polynomial in the number of processors for small values of $|s-t|$. In [2.2] he provided a polynomial time algorithm for $t/t+1$ diagnosis. In another work [2.3] he defined a new class of systems called $t-1$ diagnosable system that allows diagnosis of all but one faulty processor, with the remaining faulty processor located in a second step. Another related work is [2.4].

With the advent of large scale multiprocessor systems, parallel processing community was interested in using the interconnection network as the test graph. But popular interconnection networks such as the hypercube have low connectivity and so allow only a small number of processors to be faulty. This led Professor KT to introduce in [2.5] a fault model based on local fault constraints which restrict the number of faulty processors around a processor and show that hypercubes allow a large number of faulty processors to be identified under this new model. This pioneering research led researchers to introduce other models such as the conditional diagnosability model. Professor KT has also contributed to conditional diagnosable systems by establishing in [2,6] [2.7] the conditional diagnosability of hypercubes and its generalization called matching composition networks under both the PMC model and the comparison model.

The need to use the interconnection network itself as the test and to allow a large number of processor to be faulty led researchers to investigate two other different approaches:

- Probabilistic diagnosis.
- Distributed algorithms that can be implemented on the interconnection network itself.

There has been a great deal of interest in applying system level diagnosis theories in practical systems. Professor KT has made significant contributions to applications in network management and VLSI testing as noted below.

2.1. Probabilistic Diagnosis and VLSI Testing:

In [2.8] [2.9] Professor KT gave two probabilistic diagnosis algorithm for VLSI testing. In [2.8] he analyzed the algorithm under negative binomial distribution to account for clustering. He showed that this algorithm can diagnosis almost all faulty units when the faults are clustered and even when the yield is low. This is the first practical application of system level diagnosis and the only algorithm for diagnosing clustered faults.

2.2 Distributed Diagnosis for Distributed Network Management:

In [2.10] Professor KT has designed a multi-level adaptive distributed diagnosis algorithm and implemented that on a real telecommunication network for management of faults in a distributed manner using the SNMP protocol. This is the most versatile distributed algorithm reported in the literature and the first application of system diagnosis theory to the networking area. Another related work is in [2.11].

References:

[2.1] Das, K. Thulasiraman and V. K. Agarwal, "[Diagnosis of \$t/s\$ -Diagnosable Systems](#)", **Journal of Circuits, Systems and Computers**, Vol. 1, No. 4, 1991, pp. 353-371. See also **3rd Intl. Workshop on Graph-Theoretic Concepts in Computer Science**, June 1990.

[2.2] Das, K. Thulasiraman and V. K. Agarwal, "[Diagnosis of \$t/t+1\$ -Diagnosable Systems](#)", **SIAM Journal on Computing**, Vol. 23, October 1994, pp. 895-905.

[2.3] K. Huang, A. Das, V. K. Agarwal and K. Thulasiraman, "A Class of 2-Step Diagnosable Systems: Degree of Diagnosability and a Diagnosis Algorithm", **IEEE International Symposium on Circuits and Systems**, 1992.

[2.4] K. Thulasiraman, K. Huang, A. Das, and V. K. Agarwal, "Correct Diagnosis of Almost All Faulty Units in a Multiprocessor System", **ISCAS 1999**.

[2.5] Das, K. Thulasiraman, V. K. Agarwal and K. B. Lakshmanan, "[Multiprocessor Fault Diagnosis Under Local Constraints](#)", **IEEE Trans. on Computers**, Vol. 42, No. 8, Aug. 1993, pp. 984-988.

[2.6] Min Xu, Krishnaiyan Thulasiraman, Qiang Zhu, "Conditional diagnosability of the class of matching composition networks under the comparison model", **Theoretical Computer Science** 674 (2017) pp 53-62.

[2.7] Min Xu, K. Thulasiraman and Xiao Dong Hu, "Conditional Diagnosability of Matching Composition Networks Under the PMC Model" **IEEE Transactions on Circuits and Systems, Part: Briefs**, Vol.56, November 2009, pp. 875-889.

[2.8] K. Huang, V.K. Agarwal and K. Thulasiraman, "[Diagnosis of Clustered Faults and Wafer Testing](#)", **IEEE Trans. on IC/CAD**, Vol. 17, Feb. 1998, pp. 136-148. See also K. Huang, V.K. Agarwal and K. Thulasiraman, "[Wafer Probing with Imperfect Comparison](#)", **Proc. Intl. Symp. on Fault Tolerant Computing**, Boston, July 1992.

[2.9] K. Huang, V.K. Agarwal and K. Thulasiraman, "[A Diagnosis Algorithm for Constant Degree Structures and Application to VLSI Circuit Testing](#)", **IEEE Trans. on Parallel and Distributed Systems**, Vol. 6, April 1995, pp. 363-372.

[2.10] Ming Shan Su and K. Thulasiraman, "A Scalable Online Multilevel Distributed Network Fault Detection/Monitoring System Based on the SNMP Protocol", **Proc. IEEE Globecom 2002**.

[2.11] C. C. Lamb, L. S. DeBrunner, A. Das, and K. Thulasiraman, "Distributed Diagnosis for Multiprocessor Systems using Extended Local Neighborhoods", **IEEE Midwest Symposium on Circuits and Systems**, August 2000.

III. Fault Tolerant Design and Analysis of Interconnection Networks

Interconnection network is the most important component of a parallel processing system connecting all the processors to facilitate communication. Graph parameters such as diameter, connectivity, and regularity capture the fault tolerance properties of the interconnection networks. In a series of papers [3.1- 3.4] Professor KT extensively contributed to this area. .

In [3.1] he gave a procedure to designing a graph with minimum number of vertices that has a specified diameter, connectivity and regularity. This work generalizes all the earlier on fault tolerant interconnection network design. In [3.2] he introduced the engineering notion of sensitivity in the design of fault tolerant networks through the concept of incremental diameter and incremental degree sequences. Using the results in this paper, a graph having a specified increase in diameter and specified maximum increase in diameter can be constructed. In [3.3] he proposed DCC linear functions which can generate highly connected regular graphs which are of significantly higher order than de Bruijn graphs.

Hypercube is the most popular and widely used interconnection network. Hypercube-like networks generalize hypercubes with more attractive properties from the point of view of fault tolerance. In his most recent work [3.4] Professor KT established several properties of hypercube-like networks such as the existence of spanning paths when edge faults occur. Professor KT also discusses in this paper how these networks could serve as logical topologies in IP-over-WDM optical networks.

In related earlier works [3.5-3.6] Professor KT studied an extremal problem in graph theory involving independence number of a graph. He gave a constructive proof of Turan's theorem by determining the maximum number of edges in a graph on n vertices with a given independence number. Turan's theorem was the first result in extremal graph theory.

References:

[3.1] V. Krishnamoorthy, K. Thulasiraman and M. N. S. Swamy, "[Minimum Order Graphs with Specified Diameter, Connectivity and Regularity](#)", *Networks Journal*, Vol. 19, 1989, pp. 24-46

[3.2] V. Krishnamoorthy, K. Thulasiraman and M. N. S. Swamy, "[Incremental Distance and Diameter Sequences of a Graph: New Measures of Network Performance](#)", *IEEE Transactions on Computers*, Vol.39, Feb. 1990, pp.230-237.

[3.3] J. Opatrny, D. Sotteau, N. Srinivasan and K. Thulasiraman, "[DCC Linear Congruential Graphs: A New Class of Interconnection Networks](#)", *IEEE Trans. Computers*, Vol. 45, Feb. 1996, pp. 156-164.

[3.4] Min Xu, Khrishsagar Naik and Krishnaiyan Thulasiraman, "Fault Tolerance of Hypercube Like Networks: Spanning Laceyability under Edge Faults" Under Review for *IEEE Transactions on Network Science and Engineering*.

[3.5] P. K. Rajan and K. Thulasiraman, "[K-Sets of a Graph and Vulnerability of Communication Nets](#)", *Matrix and Tensor Quarterly*, 1974, pp.63-66.

[3.6] P. K. Rajan and K. Thulasiraman, "[K-Sets of a Graph and Vulnerability of Communication Nets](#)", *Matrix and Tensor Quarterly*, 1974, pp.77-86.

IV. Survivability in Optical Communication Networks: Protection and Restoration in Optical Infrastructure and Logical Topology Survivability in IP-Over-WDM Optical Networks

Professor KT has extensive contributions to survivability problems that arise in the study of optical communication networks. In this area availability of disjoint trees and paths play a very critical role and Professor KT's works address several issues and provided unifying schemes for these problems.

4.1. Protection and Restoration in Optical Infrastructure

In the context of survivable routing in optical communication networks Medard, Finn, Barry and Gallager presented a scheme (called MFBG scheme) to construct a pair of redundant directed spanning trees from a root node in such a fashion that the failure of any node or edge in the graph other than the root node leaves each vertex connected to the root by one of the directed trees, provided the network is 2-edge connected or 2-vertex connected. These trees are called red and blue trees. In [4.1] Professor KT presented a generalization of MFBG scheme called G-MFBG that

generates red and blue trees that cannot be generated by the MFBG scheme. Further he presented heuristics that generate red and blue trees that have very good quality of service (QoS) and quality of protection (QoP) properties. In [4.2] [4.3] he presented linear time algorithms to generate red and blue trees with high QoS and high QoP for protection against single link failure, and another linear time algorithm for generating red and blue trees with high QoS for protection against a single node failure. Using simulations it has been shown that these schemes outperform those available in the literature.

4.2 Disjoint Paths in Optical Infrastructure

Constructing disjoint paths is an important requirement in the protection and restoration of optical networks. In [4.4] Professor KT presented an algorithm to establish a set of disjoint light paths on a tree topology using single wavelength to maximize the total traffic supported by the chosen light paths. This algorithm has worst case complexity of $O(n^3)$ where n is the number of nodes in the network. In a related work [4.5] he gave a polynomial time algorithm for constructing disjoint paths in a class of networks called minimum failure WDM Optical Networks.

4.3 Logical Topology Survivability in IP-Over-WDM Optical Networks

An IP-Over-WDM optical network is a two-layer network with the physical topology G_p representing the optical network at the lower level and the logical topology G_l representing the IP layer at the higher level. The logical topology has the same vertex set as the physical topology. Each link (i, j) in the topology is routed through a path called light path from the node i to node j in the physical topology. Failure of a physical link may disconnect several logical links. The survivable logical topology (SLTM) problem is to assign each logical link to a light path in the physical topology such that the failure of a physical link does not disconnect the logical topology. It is assumed that the logical topology is 2-connected. Assigning disjoint paths to the logical links will solve the problem. But finding such paths in the physical topology is impossible to accomplish. Two directions of research have been pursued in the literature: Structural approach and the mathematical programming approach.

4.3.1 Structural Approach: Circuits/Cut sets Duality and a Unified Algorithmic Framework

The SMART algorithmic framework proposed by Kurant and Thiran is based on repeated selection of a circuit in the logical topology mapping the links in the circuit into disjoint light paths and contractions of the links in the circuit until the entire logical topology shrinks to a single node. Circuits and cutsets are dual concepts. Similarly, contraction of a link and deleting the link are dual concepts. This duality has been extensively used in the literature to develop profound results in electrical circuit theory as well as discrete optimization on networks. In [4.6-4.8] Professor KT has presented a unified theory and algorithmic framework for the SLTM problem. This resulted in four algorithmic frameworks as special cases which include all the currently available schemes. Professor KT has also analysed these schemes with respect to their ability to provide survivability against multiple physical link failures. This work is the most profound application of duality theory outside of electrical circuit theory and network flow theory. In [4.9] Professor KT has also given schemes to augment a logical topology with new edges such that the new topology is guaranteed to admit a survivable mapping.

4.3.2 Mathematical Programming Formulations

The SLTM problem is known to be NP-complete. So all the algorithms developed for this problem are approximation algorithms. So, mathematical programming formulations have been considered in the literature. In [4.10-4.12] Professor KT has presented the most complete works on the mathematical programming formulations on the SLTM problem. In [4.10] he introduced the concept of protection spanning trees and a formulation based on these concepts. He has also provided a column generation approach for solving this mathematical programming formulation. In [4.11, 4.12] he presented formulations to generate survivable routings satisfying different metrics. He has also shown in [4.13] how protection spanning trees can be used to generate survivable mappings that survive multiple physical link failures.

Professor KT has published several other works [4.14-4.19] that considered other issues related to the SLTM problem. For example, he introduced and studied in [4.17-4.19] the concept of dominator sequences in bipartite

graphs that arises in the concept of the algorithmic approach discussed in section 4.3 the most complete and comprehensive work on this problem.

References:

- [4.1] Guoliang Xue, Li Chen and K. Thulasiraman, "[*Quality of Service and Quality of Protection Issues in Preplanned recovery Schemes using Redundant Trees*](#)" **IEEE Journal of Selected Areas in Communication (JSAC)**, Vol.21, October 2003, pp. 13432-1345.
- [4.2] Weiyi Zhang, Guoliang Xue, Jiang Tang and K. Thulasiraman, "Linear Time Construction of Redundant Trees for Recovery Schemes Enhancing QoP and QoS", **INFOCOM 2005**, Miami, March 2005.
- [4.3] Weiyi Zhang, Guoliang Xue, Jian Tang and Krishnaiyan Thulasiraman, "Faster", **IEEE/ACM Transactions on Networking**, June 2008, pp.642-655.
- [4.4] Weiyi Zhang, Jian Tang, and Krishnaiyan Thulasiraman, "An Improved Algorithm for Optimal Lightpath Establishment on a Tree Topology", **IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS**, VOL. 24, NO. 8, AUGUST 2006.
- [4.5] Guoliang Xue, Ravi Gottapu , Xi Fang , Dejun Yang and K. Thulasiraman, " A Polynomial Time Algorithm for Computing Disjoint Lightpaths in Minimum Isolated-F failure Immune WDM Optical Networks", **IEEE/ACM Trans. Networking** , Vol. 22, April, 2014, pp, 470-483.
- [4.6] K. Thulasiraman, Muhammad Javed and Guoliang Xue, "Circuits/Cutsets Duality: A Unified Algorithmic Framework for Survivable Logical Topology Design in IP Over wdm Optical Networks", **IEEE INFOCOM, 2009**.
- [4.7] Krishnaiyan Thulasiraman, Muhammad Javed and Guoliang (Larry) Xue, "Primal Meets Dual: A Generalized Theory of Logical Topology Survivability in IP-over-WDM Optical Networks", **Second International Conference on Communication Systems and Networks, Jan. 2010**.
- [4.8] K. Thulasiraman, Tachun Lin and Zhili Zhou, "Robustness of Logical Topology Mapping Algorithms for Survivability against Multiple Failures in an IP Over WDM Optical Networks", **IEEE International Conference on Communication Systems and Networks (COMSNETS), 2012**.
- [4.9] Krishnaiyan Thulasiraman, Tachun Lin, M. Javed, and Guoliang. Xue, "Logical Topology Augmentation for Guaranteed Survivability under Multiple Failures in IP-over-WDM Optical Networks", **Optical Switching and Networking (OSN) journal Special Issue of Advanced Networks and Telecom. Systems**, Vol. 7, Dec. 2010, pp. 2016-214.
- [4.10] Zhili Zhou, Tachun Lin, K. Thulasiraman and Guoliang Xue, " Novel Survivable Logical Topology Routing in an IP Over WDM Optical Network based on the Logical Protection Spanning Tree Set,' **IEEE/ACM Transactions on Networking**, Vo. 25, June 2017, pp. 1673-1685.**ALSO in IEEE International Workshop on Network Design and Modeling (RNDM), 2012. (Runner UP for the Best Paper Award)**.
- [4.11] Tachun Lin, Zhili Zhou, K. Thulasiraman, Guoliang Xue an Sartaj Sahni, "Unified Mathematical Programming Frameworks for Survivable Logical Topology Mapping in IP Over WDM Optical Networks"", **IEEE/OSA Journal of Optical Communication and Networks**, VOL. 6, NO. 2 February, 2014 (pp.190- 203).
- [4.12] Zhili Zhou, Tachun Lin, K. Thulasiraman, Guoliang Xue and Sartaj Sahni, " Cross Layer Survivability in Layered Networks under Multiple Cross Layer Metrics", **IEEE/OSA Journal; of Optical Communication and Networks**, VOL. 7, June, 2015 (pp.540- 553).
- [4.13] Zhili Zhou, Tachun Lin, and Krishnaiyan Thulasiraman, "Survivable Cloud Network Design Against Multiple Failures Through Protecting Spanning Trees," **IEEE/OSA Journal of Lightwave Technology (JLT)**, Vol. 35, No. 2, Jan. 2017 (pp. 288 - 298).

[4.14] Muhammad Javed, Krishnaiyan Thulasiraman and Guoliang (Larry) Xue, "Logical Topology Design for IP-over-WDM Networks: A Hybrid Approach for Minimum Protection Capacity", ICCCN, Aug. 2008.

[4.15] Guoliang Xue, Weiyi Zhang, Tie Wang, and Krishnaiyan Thulasiraman, "[On the Partial path Protection Scheme for WDM Optical Networks and Polynomial Time Computability of Primary and Secondary Paths](#)", Journal of Industrial and Management Optimization, Vol. 3, No. 4, Nov. 2007.

[4.16] Muhammad Javed, Krishnaiyan Thulasiraman and Guoliang (Larry) Xue, "[Lightpaths Routing for Single Link Failure Survivability in IP-over-WDM Networks](#)", Journal Of Communication and Networks. Dec. 2007 9:394-

[4.17] B. Jayaram, S. Arumugam and K. Thulasiraman, "Dominator Sequences in Bipartite Graphs", Theoretical Computer Science, Vol 694, September 2017, pp. 34-41.

[4.18] B. Jayaram, S. Arumugam and K. Thulasiraman, "Independent Dominant Sequence in Bipartite Graphs", Procedia Computer Science Elsevier Publishing Company, December 2015. Volume 74, 2015, Pages 43-46.

V. Identifying Codes for Fault Identification in Sensor Networks

Consider an undirected graph G with vertex set V and edge set E . A ball of radius $t \geq 1$ centered at a vertex v is defined as the set of all vertices that are at distance t or less from v . The vertex v is said to cover itself and all the vertices in the ball with v as the center. The identifying codes problem defined by Karpovsky et al. is to find a minimum set D such that every vertex in G belongs to a unique set of balls of radius $t \geq 1$ centered at the vertices in D . The set D may be viewed as a code identifying the vertices and is called an identifying set.

Consider a communication network modeled as an undirected graph G . Each vertex in the graph represents a processor and each edge represents the communication link connecting the processors represented by the end vertices. Some of the processors could become faulty. To simplify the presentation let us assume that at most one processor could become faulty at any given time. Assume that a processor, when it becomes faulty, can trigger an alarm placed on an adjacent processor. We would like to place alarms on certain processors that will facilitate unique identification of the faulty processors. We would also like to place alarms on as few processors as possible. If D is a minimum identifying set for the case $t = 1$, then placing alarms on the processors represented by the vertices in the set D will help us to uniquely identify the faulty processor. Notice that we only need to consider $t = 1$ because if $t > 1$ is desired, we can proceed with G_t the t th power of G .

It has been shown that unique identification of vertices may not always be possible for certain topologies. In other words, triggering of alarms on a set of processors could mean that one of several candidate processors could be faulty. To alleviate this Professor KT introduced in [5.1] the d -identifying codes problem and proposed approximation schemes based on entropy concepts from information theory and analyzed its effectiveness on random graphs. This generalization is similar to the introduction of t 's diagnosable systems that generalize the t -diagnosable systems introduced by Preparata, Metze and Chien and discussed in section II.

The entropy based scheme provides a new paradigm for approximation algorithm design for certain classes of combinatorial optimization problem.

Professor KT [5.2][5.3] has also studied the identifying codes problem for certain classes of graphs.

In a related work [5.4] Professor KT gave an algorithm for coding undirected graphs.

References:

- [5.1] Ying Xiao, C. Hadjicostis, and K.Thulasiraman, "The d-Identifying Codes Problem for Vertex Identification in Graphs: Probabilistic Analysis and an Approximation Algorithm", **COCOON 2006** (12th Annual International Computing and Combinatorics Conference), Taipei, August 2006.
- [5.2] Xu, Krishnaiyan Thulasiraman and Xiao-Dong Hu, "[*Identifying Codes of Cycles of Odd orders*](#)" **European Journal of Combinatorics**, February 2008, pp.1717-1720..
- [5.3] K. Thulasiraman, Min Xu, Ying Xiao and Xiaodong Hu, "Vertex Identifying Codes for Fault Isolation in Communication Networks", Proceedings of the International Conference on Discrete Mathematics and Applications (**ICDM 2006**), Bangalore, December 2006.
- [5.4] K. N. Venkataraman and K. Thulasiraman, "An Algorithm for Coding Undirected Graphs", **IEEE International Symposium on Information Theory**, Cornell University, August 1977.

TRAFFIC ENGINEERING: ROUTING, PROTOCOL TESTING AND TOPOLOGY ABSTRACTION SERVICE

VI. Quality of Service (QoS) Routing in Communication Networks

QoS routing is a fundamental problems in several applications including fault tolerance communication networks. QoS routing requires minimum cost paths that also satisfy certain additional constraints on link metrics. This can be formulated as an integer linear programming problem. Professor KT has contributed the following versions of this problem versions of this problem. Professor KT has given computationally efficient algorithms by applying primal and dual methods of the simplex method on relaxed versions of the problems. He has also given polynomial time approximation algorithms for multi-constrained route selection. In addition, he has given approximation schemes to compute a most probable delay constrained path:

- Constrained single source to single destination shortest path : Dual Method [6.1]
- Constrained single source to single destination shortest path : Primal Method [6.2]
- Constrained disjoint single source to single destination shortest paths [6.3]
- Multi-constrained single source to single destination shortest paths Dual Method [6.4]
- Multi-constrained single source to single destination shortest paths Approximation algorithms [6.5][6.6]
- Most probable delay constrained path: [6.7]
- A US Patent on delay constrained shortest path [6.8]

References:

- [6.1]Ying Xiao, K. Thulasiraman and Guoliang Xue, "[*The Constrained Shortest Path Problem: Algorithmic Approaches and an Algebraic Study with Generalization*](#)" **AKCE International Journal of Graphs and Combinatorics** 2, No 2 pp. 63-86, Nov 2005.
- [6. 2] Ying Xiao, Krishnaiyan Thulasiraman and Guoliang Xue, "[*QoS Routing in Communication Networks: Approximation Algorithms Based on the Primal Simplex Method of Linear Programming*](#)", **IEEE Transactions on Computers**, July 2006.
- [6.3] Ying Xiao, K. Thulasiraman and Guoliang Xue, "[*Constrained Shortest Link-Disjoint Paths Selection: A Network Programming Based Approach*](#)" ,**IEEE Transactions in Circuits and Systems**, Vol 53, May 2006, pp 1174-1187.

[6.4] Ying Xiao, K. Thulasiraman, Guoliang Xue and Mamta Yadav, "QoS Routing under Multiple Additive Constraints: A Generalization of the LARAC Algorithm " **IEEE Transactions on Emerging topics in Computing**, June 2015. April 2016, pp .242-253.

[6.5] Guoliang Xue, Weiyi Zhang, Jian Tang and Krishnaiya Thulasiraman, "Polynomial", **IEEE/ACM Transactions on Networking**, June 2008, pp.656-669.

[6.6] Guoliang Xue, Arunabha Sen, Weiyi Zhang, Jian Tang, and Krishnaiyan Thulasiraman, "[Finding a path subject to many additive QoS constraints](#)" **IEEE/ACM Transactions on Networking**, Vol. 15, February, 2007, pp.201- 211.

[6.7] Y. Xiao, K. Thulasiraman, Xi Fang, D.Wang and G. Xue, "Computing a Most Probable Delay Constrained Path: NP-Hardness and Approximation Schemes" **IEEE Trans. Computers**, Vol.61, May 2012, pp. 738-744.

[6.8] Ravi Ravindran, Guo-Qiang Wang and Krishnaiyan Thulasiraman, "Distributed Quality of Service Routing" U.S. Patent #7,499,404, March 2009.

VII. Conformance Testing of Communication Protocols

Conformance testing of a communication protocol is intended to ensure that a given implementation of a protocol is equivalent to the standard specification of the protocol. The quality of internetworking among heterogeneous subsystems in a distributed system can be assured through the conformance testing of each subsystem. The testing involves selection of a test suite from the specification and execution of the test suite on the implementation under a specific test environment. Professor KT has made extensive contributions to the suite selection methods for testing the control flow aspects of protocols represented as Finite State Machines (FSM).

The minimum length test sequence generation method called the U-method for conformance testing uses Unique Input Sequence (UIS) for state identification. In the MU method it is assumed that multiple UIS's are assumed to be available for each state. Both these methods require that the test graph be connected. This raises an important question: Does there exist an assignment of UIS's to the transitions such that the resulting test graph is connected. In [7.1] Professor KT formulated this problem as a maximum matroid 2-intersection problem and discussed an efficient algorithmic solution. This is called the BUAP algorithm. This is the first application of matroid theory to an engineering problem outside electrical circuit theory.

In [7.2] Professor KT carried out an analysis of the fault diagnosis capabilities of various FSM based test selection methods and concluded that the Wp method has the best fault resolution capability. But the Wp method suffers from lack of certain properties desirable for fault diagnosis. So Professor KT proceeded to find in [7.2] a method better than the Wp method.

In [7.3] Professor generalized the MU-method using the BUAP algorithm and the rural Chinese postman problem. This new method is applicable to all protocols that have at least one UIO sequence whereas the U- method and the MU-method are applicable for only a subset of these protocols.

In [7.4] Professor KT has given a comprehensive review of several test sequence selection methods for the conformance testing of protocols modeled as FSMs.

In a sequence of two papers Professor KT studied the test selection problem for protocols modeled as Extended Finite State Machines[EFSM]. In [7.5] he introduced the concept of context independent unique sequences. In [7.6] he presented a unified test case generation method for testing the control flow and data flow aspects of a protocol modeled as EFSMs.

References:

- [7.1] T. Ramalingam, A. Das and K. Thulasiraman, "[A Matroid-Theoretic Solution to an Assignment Problem in Communication Protocol Testing](#)", IEEE Trans. on Computers, 49(4):317-330, April 2000.
- [7.2] T. Ramalingam, K. Thulasiraman and A. Das, "[On Testing and Diagnosis of Communication Protocols Based on the FSM Model](#)", Computer Communications, Vol. 18, No. 5, 1995, pp. 329-337.
- [7.3] Ramalingam, A. Das and K. Thulasiraman, "A Generalization of the Multiple UIO-Sequence Method of Test Selection for FSM-Based Protocols", International Workshop on Protocol Test Systems, Tokyo, November 1994, pp. 209-224.
- [7.4] T. Ramalingam, K. Thulasiraman and A. Das, "[Fault Detection and Diagnosis Capabilities of Test Selection Methods for FSM-Based Protocols](#)", Computer Communications, Vol. 18, No. 2, 1995, pp. 113-122.
- [7.5]. Ramalingam, K. Thulasiraman and A. Das, "[Context Independent Unique State Identification Sequences for Testing Communication Protocols Modeled as Extended Finite State Machines](#)" Computer Communication, Vol. 18, No. 5, 1995, pp. 329-337.
- [7.6] T. Ramalingam, A. Das and K. Thulasiraman, "A Generalization of the Multiple UIO-Sequence Method of Test Selection for FSM-Based Protocols", International Workshop on Protocol Test Systems, Tokyo, November 1994, pp. 209-224.

VIII. Topology Abstraction Service for IP VPNs

In [8.1, 8.2]] Professor KT introduced the notion of topology abstraction (TA) service to enable a VSP to share its core topology information with the VPNs. TA service is both practical and scalable in the context of managed IP-VPNs. TA service provides tunable visibility of state of the VSP's network leading to better VPN performance. A key challenge of the TA service is to generate TA with relevant network resource information for each VPN in an accurate and fair manner. In [8.3] Professor KT developed three decentralized schemes for generating TAs with different performance characteristics. These schemes used some very powerful tools from graph theory and combinatorial optimization. They achieve improved call performance, fair resource sharing for VPNs, and higher network utilization for the VSP. The idea of the VPN TA service and the performance of the proposed techniques was validated using various simulation scenarios over several topologies.

In the decentralized schemes of [8.3] it is assumed that that all the border nodes of VPNs performing the abstractions have access to the entire core network topology. This assumption likely leads to over- or under-subscription. In [8.4,8.5] Professor KT developed centralized schemes to partition the core network capacities, and assign each partition to a specific VPN for applying the decentralized abstraction schemes presented in [8.3]. First, he presented two schemes based on the maximum concurrent flow and the maximum multi-commodity flow (MMCF) formulations. He then proposed approaches to address the fairness concerns that arise when MMCF formulation is used. Through extensive simulations on several topologies and under different scenarios, it was demonstrated that core partitioning strategy leads to much better abstractions of the VPNs.

The topology considered in [8.3,8.4] for abstraction is very simple and sparse. In [8.6] Professor KT proposed two new schemes for topology abstraction. Specifically, given a core network with node set V , and also given the node-to-node maximum flow matrix $F = [f(u, v)]$ for any connected graph $G = (V^*, E)$ with V^* a subset of V , it is shown how to assign capacities to the edges of G such that the maximum available flow between any pair of vertices $u, v \in V^*$ in G is at most the maximum available flow between u and v in the core network. Though this methodology is applicable to any graph, it is desirable to have abstract topologies with certain other desirable properties: such as low degree, number of edges being linear in the number of vertices, amenable to survivable logical topology routing in an IP over WDM optical networks etc. Chordal graphs have such properties. In [8, 6] Professor KT showed how to construct 2-vertex and 2-edge connected chordal graphs, starting from the Gomory-Hu tree of the flow matrix of the core network. Using the theory of graph augmentation presented in [4, 9] one can develop other sparse virtual topologies possessing the properties demanded by an application.

References:

- [8.1] Ravi Ravindran Changcheng Huang and K. Thulasiraman, "Topology Abstraction as VPN Service", ICC 2005, Seoul, May 2005.
- [8.2] Ravi S. Ravindran, C. Huang, K.Thulasiraman, "A Dynamic Managed VPN Service: Architecture and Algorithms", ICC International Conference on Communications 2006.
- [8.3] Ravi Ravindran, Changchen Huang, and K. Thulasiraman, "Topology Abstraction Service for IP VPNs" IEEE Trans. on Parallel and Distributed Systems. Jan. 2013 (vol. 24 no. 1), pp. 184-197.
- [8.4] Ravishankar Ravindran, Changcheng Huang and Krishnaiyan Thulasiraman, "VPN Topology Abstraction Service using Centralized Core Capacity Sharing Scheme", IEEE ANTS 2009, Dec. 2009.
- [8.5] Ravishankar Ravindran, Chancheng Huang, Krishnaiyan Thulasiraman and Tachun Lin, "Topology Abstraction Service for IP VPNs: Core Network Partitioning for Resourcing" American Journal of Operations Research. arXiv:1608.04411v1 [cs.NI]
- [8. 6 Lavanya, B. Jayaram , S, Arumugam and K. Thulasiraman, "Virtual Topologies for Abstraction Service for IP VPNs" Networks 2016, Montreal, September 26-28, 2016.

MARKED GRAPHS AND DESIGN F DISTRIBUTED ALGORITHMS

IX. Reachability in Marked Graphs

A Petri net is a general algebraic structure originally developed Carl Adam Petri as a model for information flow in systems that exhibit asynchronism and parallelism. The generality of Petri nets makes modelling of large systems possible. But the feasibility of analysis becomes questionable and most often the problems are NP-complete. Marked graphs are a special class of Petri nets that are more amenable to analysis and possess enough power to model complex parallel processing systems, queuing networks etc.

A marked graph is a directed graph in which each edge is associated with a nonnegative integer value called token. The set of all tokens on all edges of the marked graph is called a marking. Firing a node is the operation of adding a token to the marking of each outgoing edge at the node, and subtracting a token from the marking of each incoming edges at the node. A fundamental problem is: given a marking M_i , determine a sequence of legal firings that takes the graph to another specified marking. In a fundamental result, Tadao Murata provided a circuit theoretic answer to this problem. Starting from this, Professor KT investigated in [9.1] the problem of determining a marking that maximizes the weighted sum of all edge tokens. This is more general than other versions of the problem considered earlier by researchers. Professor KT studied this using a linear programming formulation and the simplex method. In the course of his analysis he pointed out interpretations of operations of simplex method in terms of marked graph concepts. For example, he introduced concepts such as diakoptic firing. While developing the ideas of his solution approach he showed using principles of duality that the problem considered is equivalent to the problem of determining the maximum marking in a computation graph when the input quantum, output quantum , and the threshold of each edge of the computation graph are 0 or 1. Professor KT also extended this study for the case of capacitated marked graphs in which the token values on edges are constrained. Finally, he showed how to handle the maximum marking problem for non-live marked graphs.

In [9.2] Professor KT, using a linear programming formulation, provided a unified treatment of the sub-marking reaching problem for both capacitated and uncapacitated cases. In both cases he showed that the problem is equivalent to testing feasibility of the dual transshipment problem of operations research. For this feasibility

problem he provided a polynomial algorithm. It should be pointed out that this work generalizes the earlier pioneering work by Kumagai, Kodama and Kitagawa.

In [9.3] Professor KT provided a purely graph theoretic characterization of the reachability problem on (0,1) capacitated marked graphs. He also pointed out a relationship between this work and that of Gafni and Bertsekas on generating loop-free routings in frequently changing topologies.

In [9.4], combining the circuit theoretic framework of Murata with the graph theoretic framework of Commonner, Holt, Even and Pnueli, Professor KT provided algorithmic solutions to several problems on marked graphs. In particular, he introduced the concept of scatter of a firing sequence and provided a minimum scatter firing sequences of several topologies.

References:

[9.1] M. A. Comeau and K. Thulasiraman, "[*Structure of the Submarking Reachability Problem and Network Programming*](#)", IEEE Transactions on Circuits and Systems, Vol. CAS-35, Jan. 1988, pp. 89-100.

[9.2] K. Thulasiraman and M. A. Comeau, "[*Structure of a Reachability Problem for \(0,1\) Capacitated Marked Graphs*](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-34, April 1987, pp. 430-431.

[9.3] K. Thulasiraman and M. A. Comeau, "[*Maximum-Weight Markings in Marked Graphs: Algorithms and Interpretations Based on the Simplex Method*](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-34, December 1987, pp. 1535-1545. Also see IEEE International Symposium on Circuits and Systems, Kyoto, Japan, June 1985.

[9.4] M. A. Comeau and K. Thulasiraman, "[*Algorithms on Marked Directed Graphs*](#)", Canadian Electrical Engg. Journal, Vol. 9, 1984, pp. 72-79.

X. Parallel and Distributed Computations on Graphs and Networks

The works outlined in Section IX triggered Professor KT's interest in parallel and distributed computation.

Noting that the legal firing operation on a node is the same as the node (dual) variable encountered in the dual simplex method of network programming, and that legal firing operations on nodes can be performed concurrently without affecting feasibility, Professor KT developed in [10.1, 10.2] two novel distributed and parallel algorithms for the transshipment problem.

In addition, Professor KT has given distributed algorithms for several fundamental graph problems that form the building blocks for design of complex distributed algorithms and also provided distributed solutions to certain fundamental techniques of interest in parallel and distributed computing. They are listed below [10.3-10.13].

- Design of synchronizers for synchronous communication
- Shortest paths
- Depth-first search
- Distributed Diagnosis and network Management

References:

- [10.1] K. Thulasiraman, R. P. Chalasani and M. A. Comeau, "Parallel Network Dual Simplex Method on a Shared Memory Multiprocessor", **Proc. 5th IEEE Symp. on Parallel and Distributed Processing**, Dallas, December 1993, pp. 408-415.
- [10.2] Danny Phelps, Ming-Shan Su and K. Thulasiraman, "Distributed Testing and Diagnosis in a Mobile Computing Environment", **IWCMC 2010**, pp. 1268-1272 Caen, France.
- [10.3] **Ming Shan Su**, "Multilevel Adaptive Distributed Diagnosis for Fault Location in a Network of Processors and Design of a Distributed Network Fault Detection System Based on the SNMP Protocol",
- [10.4] **K. Thulasiraman, Ming Shan Su and Vakul Goel**, "The Multilevel Paradigm for Distributed Fault Location in Networks with Unreliable Processors", ISCAS 2003, Thailand.
- [10.5] **C. C. Lamb, L. S. DeBrunner, A. Das, and K. Thulasiraman**, "Distributed Diagnosis for Multiprocessor Systems using Extended Local Neighborhoods", **IEEE Midwest Symposium on Circuits and Systems**, August 2000
- [10.6] **K. Thulasiraman, A. Das and V. K. Agrawal**, "[*Distributed Fault Diagnosis of a Ring of Processors*](#)", **Parallel Processing Letters**, Vol. 3, No. 2, 1993, pp. 195-204
- [10.7] **S. Srinivas, K. Thulasiraman and M.N.S. Swamy**, "[*A MIN-based Reconfigurable Architecture for de Bruijn Structures*](#)", **International Journal of High Speed Electronics**, Vol. 3, 1992, pp. 279-296.
- [10.8] **K. B. Lakshmanan, N. Meenakshi and K. Thulasiraman**, "[*A Time-Optimal Message-Efficient Distributed Algorithm for Depth-First Search*](#)", **Information Processing Letters**, Vol. 25, No. 2, May 1987, pp. 103-109.
- [10.9] **K. B. Lakshmanan and K. Thulasiraman**, "On the Use of Synchronizers for Asynchronous Communication Networks", **Workshop on Distributed Algorithms**, Amsterdam July 1987
- [10.10] **Y. Kajitani, H. Miyano, S. Ueno, and K. Thulasiraman**, "On the Optimal Synchronizer for Asynchronous Distributed Networks", **Proc. Tech. Group on CAS, IEICE**, Nov 1988.
- [10.11] **M. A. Comeau, K. Thulasiraman and K. B. Lakshmanan**, "An Efficient Asynchronous Distributed Protocol to Test Feasibility of the Dual Transshipment Problem", **25th Allerton Conference on Communication, Control and Computing**, University of Illinois, Urbana- Campaign, September 1987
- [10.12] **M. Toulouse, T. Crainic, and K. Thulasiraman**, "[*Global Optimization Properties of Parallel Cooperative Search Algorithms: A Simulation study*](#)", **Parallel Computing**, Vol. 26, 2000, pp. 91-92.
- [10.13] **K. B. Lakshmanan and K. Thulasiraman**, "On the Use of Synchronizers for Asynchronous Communication Networks", **Workshop on Distributed Algorithms**, Amsterdam July 1987.

VERY LARGE SCALE INTEGRATED CIRCUITS

XI. Computer Aided Design of VLSI Circuits

Graph and combinatorial optimization algorithms play a central role in the design of tools for VLSI Circuits. Professor KT has contributed a variety of algorithms to this area. They are [11.1-11.15].

- Planar Layout
- Graph Planarization
- Channel Routing
- Switch Box Routing
- Parallel CAD: Layout Compaction and Wire Length Minimization
- Floor Planar Design
- Graph Partitioning
- Enumeration Problems on Graphs
- VLSI Testing

References:

[11.1] R. Jayakumar, K. Thulasiraman and M. N. S. Swamy, "[O\(N²\) Algorithms for Graph Planarization](#)", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. CAD-8, March, 1989, pp. 257-267.

[11.2] K. Thulasiraman, R. Jayakumar and M. N. S. Swamy, "[Planar Embedding: Linear-Time Algorithms for Vertex Placement and Edge Ordering](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-35, March 1988, pp. 334-344.

[11.3] M. Kaufmann, S. Gao, and K. Thulasiraman, "[An Algorithm for Steiner Trees in Grid Graphs and its Application to Homotopic Routing](#)", Journal of Circuits, Systems and Computers. Vol. 6, 1996, pp. 1-14.

[11.4] J. Lienig and K. Thulasiraman, "[GASBOR: A New Genetic Algorithm for Switch-Box Routing in Integrated Circuits](#)", Journal of Circuits, Systems and Computers. Vol. 6, 1996, pp. 356-373. See also J. Lienig and K. Thulasiraman, "[GASBOR: A Genetic Algorithm for Switch-Box Routing in Integrated Circuits](#)", Proc. AI '94 Workshop on Evolutionary Computation, Armidale, Australia, 1994, pp. 199-212.

[11.5] R. P. Chalasani, K. Thulasiraman and M. A. Comeau, "Integrated VLSI Layout Computation and Wire Balancing on a Shared Memory Multiprocessor: Evaluation of a Parallel Algorithm", Proc. **International Symp. on Parallel Architectures, Algorithms and Networks, (ISPAN)**, December, 1994, Kanazawa, Japan, pp. 49-56.

[11.6] M. K. Kaufmann, S. Gao and K. Thulasiraman, "On Steiner Minimal Trees in Grid Graphs and Its Application to VLSI Routing", Proc. **5th Intl. Symposium on Algorithms and Computations**, 1994, pp. 351-359.

[11.7] J. Lienig and K. Thulasiraman, "[A Genetic Algorithm for Channel Routing in VLSI Circuits](#)", Evolutionary Computation, Vol. 1, No. 4, 1994, pp. 293-331. [Also see Proc. Seventh Intl. Conf. on VLSI Design](#), Calcutta, January 1994, pp. 133-136.

[11.8] K. Thulasiraman, R. P. Chalasani, P. Thulasiraman and M. A. Comeau, "Parallel Network Primal-Dual Method on a Shared Memory Multiprocessor and A Unified Approach to VLSI Lay-out Compaction and Wire Balancing", Proc. **IEEE VLSI Design '93**, Bombay, Jan. 1993.

[11.9] Safir, B. Haroun and K. Thulasiraman, "A Floorplanner Driven by Structural and Timing Constraints", Proc. **IEEE Intl. Symp. Circuits and Systems**, London, May 1994.

[11.10] J. Lienig, K. Thulasiraman and M.N.S. Swamy, "Routing Algorithms for Multi-Chip Modules", Proc. **European Design Automation Conf.**, Hamburg, 1992, pp. 286-291.

[11.11] Quyang, M. Toulouse, K. Thulasiraman, F. Glover, and J. S. Deogun, "[Multilevel Cooperative Search for the Circuit/Hypergraph Partitioning Problem](#)", IEEE Trans. on CAD of Integrated Circuits and Systems, vol.21, June 2002, pp. 685-693. See also M. Toulouse,

[11.12] K. Thulasiraman and F. Glover, "[Multi-Level Cooperative Search: A New Paradigm for Combinatorial Optimization and an Application to Graph Partitioning](#)", International European Parallel Processing Conference, Vol. 1685, Lecture Notes in Computer Science, 1999, pp. 533-542.

[11.13] Y. Zhao, L. Tao, K. Thulasiraman and M.N.S. Swamy, "[Simulated Annealing and Tabu Search Algorithms for Multiway Graph Partition](#)", Journal of Circuits, Systems and Computers, Vol. 2, No. 2, 1992, pp. 159-185.

[11.14] Dong Xiang, Kaiwei Li, Hideo Fujiwara and Krishnaiyan Thulasiraman, "[Constraining Transition Propagation for Low Power Scan Testing Using a Two-Stage Scan Architecture](#)", IEEE Transactions on Circuits and Systems, Part II: Briefs, May 2007, pp. 450-454.

[11.15] Dong Xiang, Jia-Guang Sun, Jie Wu and Krishnaiyan Thulasiraman, "Fault Tolerant Routing in Meshes/Tori Using Planarly Constructed Fault Blocks", ICCP 2005, Oslo.

XII. Graph Theory

In the course of his research employing graph theory and algorithms as analytical tools, Professor KT has also introduced new graph theoretic concepts and related algorithms [12.1- 12.7]. Certain publications from some of the other sections whose primary focus is of a graph theoretic nature are also listed below.

References:

[12.1] Guoliang Xue and K. Thulasiraman, "[Computing Shortest Network under Fixed Topology](#)" IEEE Transactions on Computers, Vol. 51, September 2002, pp. 1117-1120.

[12.2] K. Thulasiraman and M. N. S. Swamy, "[A Theorem in the Theory of Determinants and the Number of Spanning Trees of a Graph](#)", Canadian Electrical Engg. Journal, Vol. 8, 1983, pp. 147-52.

[12.3] K. Thulasiraman, P. S. Reddy and M. G. G. Naidu, "[Similarity of Graphs and Enumeration of Distinct nth Order Symmetric Sign Patterns](#)", Canadian Electrical Engineering Journal, Vol. 10, Jan. 1985, pp. 9-14. See also Proc. IEEE Intl. Symp. on Circuits and Systems, Rome, 1983.

[12.4] R. Jayakumar, K. Thulasiraman and M. N. S. Swamy, "[Complexity of Computation of a Spanning Tree Enumeration Algorithm](#)", IEEE Transactions on Circuits and Systems, Vol. CAS-31, October 1984, pp.853-860.

[12.5] R. Jayakumar, K. Thulasiraman and M. N. S. Swamy, "[MOD-CHAR: An Implementation of Char's Spanning Tree Enumeration Algorithm and its Complexity Analysis](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-36, Feb. 1989, pp. 219-228.

[12.6] K. Thulasiraman, R. Jayakumar and M. N. S. Swamy, "[On Maximal Planarization of Non-Planar Graphs](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-33, Aug. 1986, pp. 843- 844. Also see K. Thulasiraman, R. Jayakumar and M. N. S. Swamy, "[An Optimal Algorithm for Maximal Planarization of Non-Planar Graphs](#)", Proc. IEEE Intl. Symp. on Circuits and Systems, San Jose, May 1986.

[12.7] K. Thulasiraman and M. A. Comeau, "[On Determining a Computable Ordering of a Digital Network](#)", Proc. IEEE, Vol. 71, November 1983, pp. 1323-1324.

Section III

- [3.1] V. Krishnamoorthy, K. Thulasiraman and M. N. S. Swamy, "*Minimum Order Graphs with Specified Diameter, Connectivity and Regularity*", Networks Journal, Vol. 19, 1989, pp. 24-46
- [3.2] V. Krishnamoorthy, K. Thulasiraman and M. N. S. Swamy, "*Incremental Distance and Diameter Sequences of a Graph: New Measures of Network Performance*", IEEE Transactions on Computers, Vol.39, Feb. 1990, pp.230-237.
- [3.3] J. Opatrny, D. Sotteau, N. Srinivasan and K. Thulasiraman, "*DCC Linear Congruential Graphs: A New Class of Interconnection Networks*", IEEE Trans. Computers, Vol. 45, Feb. 1996, pp. 156-164.
- [3.4] Min Xu, Khrishsagar Naik and Krishnaiyan Thulasiraman, "Fault Tolerance of Hypercube Like Networks: Spanning Laceability under Edge Faults" Under Review for IEEE Transactions on Network Science and Engineering.
- [3.5] P. K. Rajan and K. Thulasiraman, "*K-Sets of a Graph and Vulnerability of Communication Nets*", Matrix and Tensor Quarterly, 1974, pp.63-66.
- [3.6] P. K. Rajan and K. Thulasiraman, "*K-Sets of a Graph and Vulnerability of Communication Nets*", Matrix and Tensor Quarterly, 1974, pp.77-86.

Section IV

- [4.17] B. Jayaram, S. Arumugam and K. Thulasiraman, "Dominators Sequences in Bipartite Graphs", Theoretical Computer Science, Vol 694, September 2017, pp. 34-41.
- [4.18] B. Jayaram, S. Arumugam and K. Thulasiraman, "Independent Dominant Sequence in Bipartite Graphs", Procedia Computer Science Elsevier Publishing Company, December 2015. Volume 74, 2015, Pages 43-46.
- [4.19] B. Jayaram, S. Lavanya, K. Thulasiraman and S. Arumugam "Maximum Dominator Sequences and Minimum Forcing Sets in Bipartite Graphs: Unifying two Seemingly Unrelated Concepts" Under Review for SIA Journal on Discrete Mathematics.

Section V

- [5.1] Ying Xiao, C. Hadjicostis, and K. Thulasiraman, "The d-Identifying Codes Problem for Vertex Identification in Graphs: Probabilistic Analysis and an Approximation Algorithm", COCOON 2006 (12th Annual International Computing and Combinatorics Conference), Taipei, August 2006.
- [5.2] Xu, Krishnaiyan Thulasiraman and Xiao-Dong Hu, "*Identifying Codes of Cycles of Odd orders*" European Journal of Combinatorics, February 2008, pp.1717-1720..
- [5.3] K. Thulasiraman, Min Xu, Ying Xiao and Xiaodong Hu, "Vertex Identifying Codes for Fault Isolation in Communication Networks", Proceedings of the International Conference on Discrete Mathematics and Applications (ICDM 2006), Bangalore, December 2006.
- [5.4] K. N. Venkataraman and K. Thulasiraman, "An Algorithm for Coding Undirected Graphs", IEEE International Symposium on Information Theory, Cornell University, August 1977.

Section XI

- [11.1] R. Jayakumar, K. Thulasiraman and M. N. S. Swamy, "*O(N²) Algorithms for Graph Planarization*", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. CAD-8, March, 1989, pp. 257-267.

- [11.2] K. Thulasiraman, R. Jayakumar and M. N. S. Swamy, "[Planar Embedding: Linear-Time Algorithms for Vertex Placement and Edge Ordering](#)", IEEE Trans. on Circuits and Systems, Vol. CAS-35, March 1988, pp. 334-344.
- [11.11] Quyang, M. Toulouse, K. Thulasiraman, F. Glover, and J. S. Deogun, "[Multilevel Cooperative Search for the Circuit/Hypergraph Partitioning Problem](#)", IEEE Trans. on CAD of Integrated Circuits and Systems, vol.21, June 2002, pp. 685-693.
- [11.13] Y. Zhao, L. Tao, K. Thulasiraman and M.N.S. Swamy, "[Simulated Annealing and Tabu Search Algorithms for Multiway Graph Partition](#)", Journal of Circuits, Systems and Computers, Vol. 2, No. 2, 1992, pp. 159-185.