Duality in graphs and logical topology survivability in layered networks

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Graphs provide natural and convenient representations of communication networks. Graph models and flow formulations have been extensively used in the study of a large number of issues relating to network analysis and design. Structural characteristics such as connectivity/fault survivability (a measure of robustness of networks when link or node failures occur) and diameter (a measure of delay incurred in transmission of information from one node to another) have served as parameters in the design of communication networks. There is a rich body of literature dealing with these and related issues.

There are two approaches to deliver telecommunication services. The first is to design a new system from scratch every time a new type or level of service is to be delivered. The second is to accomplish the desired goal using the resources available in the existing systems. The latter approach involves the concept of layering. Modern communication networks are designed using the layered approach. Typically, design using the layered approach involves mapping a guest graph (called a *logical topology*) onto a host graph (called the *physical topology*) satisfying certain requirements. For example, in *Wavelength Division Multiplexing* (WDM) based networks the physical topology is defined by a set of nodes and optical fibers connecting the nodes, and the logical topology is defined by a subset of nodes (for example, IP routers) and the lightpaths connecting these nodes in the physical topology. Thus each logical link represents a lightpath in the physical topology. This talk is concerned with survivability of the logical topology when physical nodes/links fail, leading to cascading failures at the logical layer.

The Survivable Logical Topology Mapping (SLTM) problem in an IP-over-WDM optical network is to map each link (u, v) in the logical topology (at the IP layer) into a lightpath between the nodes u and v in the physical topology (at the optical layer) such that failure of a physical link does not cause the logical topology to become disconnected. It is assumed that both the physical and logical topologies are 2-edge connected (in short, two-connected).

The problem of finding pair-wise (mutually) disjoint paths plays an important role in finding survivable mappings. This problem is well studied and is NP-complete in general [1]. However, it is possible to find pair-wise disjoint paths in some special cases e.g. when the topology is undirected three edge-connected and the number of pair-wise disjoint paths required is two [2].

In [3], Modiano and Narula-Tam formally showed that the problem of finding survivable mappings is NP-complete for general as well as for ring logical topologies. Therefore, they provided *Integer Linear Programs* (ILPs) to find a solution. The ILP is based on the observation that a logical topology can get disconnected after the failure of a physical link only if the physical link carries an entire cut of the logical topology, or alternatively, every cut of the logical topology must contain at least a pair of edges with pair-wise disjoint mappings in order for the mappings to be survivable. However, the ILP does not scale well as it must examine all the possible cuts, a number that grow exponentially with the size of the topology. Some of the other related works on this problem may be found in [4, 5].

In [6, 7, 8] Kurant and Thiran provided a framework called SMART (*Survivable Mapping Algorithm by Ring Trimming*). SMART utilizes circuits to find survivable mappings for logical topologies. The framework repeatedly picks connected pieces (subgraphs) of the logical topology and finds survivable mappings for these pieces. If a survivable mapping is found for a piece, its links are short-circuited (contracted) and the algorithm proceeds by picking another piece. The process is repeated until the logical topology is reduced to a single node or a search for a piece with survivable mapping is unsuccessful. In the former case, a survivable mapping for the logical topology has been found; otherwise a survivable mapping does not exist.

Duality between circuits and cuts in a graph is one of the well studied topics in graph theory. This concept has played a significant role in the development of methodologies for solving problems in various applications. Most of the early results in electrical circuit theory were founded on the duality relationship between circuits and cuts [9]. There is a wealth of literature on the role of duality in network optimization (that is, discrete optimization on graphs and networks) [10]. Most often, for a primal algorithm based on circuits there is a dual algorithm based on cuts for the same problem. The primal and dual algorithms possess certain characteristics that make one superior to the other depending on the application. SMART algorithm for the survivable logical topology design problem is based on circuits [6, 7, 8].

The question then arises whether there exists a dual methodology based on cuts. The work in [11] answered this question in the affirmative and provided a unified algorithmic framework for the SLTM problem. The work also provides much insight into the structure of solutions for the SLTM problem.

Effectiveness of both these frameworks—SMART and its dual— as well as their robustness in providing survivability against multiple failures depends on the lengths of the cutset cover and circuit cover sequences on which they are based. In a recent unpublished work [12] we considered these issues and developed a generalized theory of logical topology survivability. We introduced the concept of generalized cutset and generalized circuit cover sequences. We showed that the distinction between the primal and dual methods disappears when the generalized sequences are used. Details of this work will be presented in the talk.

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