

$(n+2)$ -Node Resistive n -Port Realizability of Y -Matrices

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Abstract—Sufficient conditions for the realization of a real symmetric matrix as the short-circuit conductance matrix of an $(n+2)$ -node resistive n -port network are established.

The properties of networks of departure and padding n -port networks are used to arrive at these results. It is shown that any $(n \times n)$ real symmetric matrix realizable by an $(n+1)$ -node n -port network can also be realized by an $(n+2)$ -node n -port network containing at most $n(n+1)/2$ conductances if all the n conductances of the corresponding $(n+1)$ -node realization N , form part of a fundamental cut-set in N with respect to the port tree of N .

I. INTRODUCTION

A CLASSIC UNSOLVED PROBLEM in network theory is the synthesis of resistive n -port networks having a specified short-circuit conductance matrix. Methods are known to test the realizability (and also to obtain the realization when it exists) of an $(n \times n)$ real symmetric matrix Y as the short-circuit conductance matrix of a resistive n -port network with $(n+1)$ -nodes [1], [2]. As regards the synthesis of n -port networks with more than $(n+1)$ nodes, the only general approach available is due to Guillemin [3]. Guillemin's approach is very useful when the port configuration is also specified. This approach requires, as a first step, the determination of the network of departure [4] N_d with respect to the given matrix Y and the specified port configuration T . Then a padding n -port network [4] N_p has to be generated so that the parallel combination N of N_d and N_p contains no negative conductances. The network N will realize the matrix Y . It can be shown [4] that the conductances of N_d can be obtained as simple linear combinations of the entries of Y . Reddy *et al.* have shown that the conductances of N_p can be expressed in terms of potential factors and certain parameters which can be directly related to the required network [4] N . In view of these relationships, it seemed that a study of N_d in conjunction with N_p would yield more insight into the properties of a realizable matrix Y . Frisch and Swaminathan [5] were the first to work along these lines and obtained the supremacy condi-

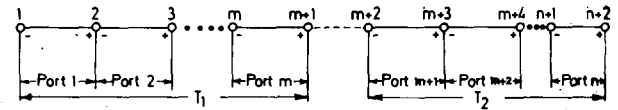


Fig. 1. Linear 2-tree port configuration.

tion. Pursuing further, Reddy and Thulasiraman obtained several conditions for $(n+2)$ -node resistive n -port networks [6].

In addition, Jambotkar and Tokad [7] have given an interesting formulation of the $(n+2)$ -node n -port problem. They have shown that the conductances of an $(n+2)$ -node n -port network N realizing a given Y -matrix can be expressed in terms of the $(n+1)$ conductances connected to any one node in N and also the entries of the matrix Y . The formulations given in [4] and [7] enable generation of continuously equivalent realizations for a given Y -matrix and minimal realizations in special cases.

In this paper we first establish, based on the results of [6], two sufficient conditions for $(n+2)$ -node realizability of Y -matrices. The condition proved in Section II is stated in terms of the entries of the matrix Y . In Section III, the realizability of uniformly tapered matrices by $(n+2)$ -node n -port networks is established. This result leads to Corollary 1, i.e., a matrix realizable by an $(n+1)$ -node n -port network with all conductances nonnegative can also be realized by an $(n+2)$ -node n -port network.

II. A SUFFICIENT CONDITION FOR $(n+2)$ -NODE REALIZABILITY OF A Y -MATRIX

Consider an $(n+2)$ -node n -port network N . Let the two connected parts T_1 and T_2 of the port configuration T of N be linear trees. Let T_0 be a linear tree of N such that $T \subset T_0$. Let the set of vertices in T_1 be denoted by V_1 and the set of vertices in T_2 by V_2 . Let the first $(m+1)$ vertices be in V_1 and the remaining $(n-m+1)$ vertices in V_2 . That is, the first m -ports will be in T_1 and the last $(n-m)$ -ports will be in T_2 . Thus the port configuration T of N will be as shown in Fig. 1, with the vertices numbered consecutively starting from one end vertex. We shall refer by g_{ij} , $(g_{ij})_d$ and $(g_{ij})_p$ the conductances connecting the vertices i and j in N , N_d , and N_p , respectively, where N_d and N_p are the network of departure and padding network of N , respectively. The conductances of N_p can be expressed as

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follows [4]:

$$(g_{ij})_p = -\frac{S_i S_j}{S}, \quad i, j \in V_1(V_2), i \neq j$$

$$(g_{ij})_p = \frac{S_i S_j}{S}, \quad i \in V_1(V_2), j \in V_2(V_1), i \neq j \quad (1)$$

where

$$S_i = \sum_{j \in V_2} (g_{ij})_p = \sum_{j \in V_2} g_{ij}, \quad i \in V_1,$$

$$S_j = \sum_{i \in V_1} (g_{ij})_p = \sum_{i \in V_1} g_{ij}, \quad j \in V_2,$$

$$S = \sum_{i \in V_1} S_i = \sum_{j \in V_2} S_j. \quad (2)$$

Let for all $i \in V_1(V_2)$ and $j \in V_2(V_1)$

$$S_{i0} = \sum_j |(g_{ij})_d|$$

for all j 's for which $(g_{ij})_d < 0$;

$$S_0 = \sum_{i \in V_1} S_{i0} = \sum_{j \in V_2} S_{j0}. \quad (3)$$

Following are the two main steps in the realization of a real symmetric matrix Y , as the short-circuit conductance matrix of an $(n+2)$ -node network having a specified port configuration T .

- 1) Determination of N_d .
- 2) Choice of nonnegative values of S_i 's so that the conductances of N_p as given by (1) satisfy the property:

$$(g_{ij})_d + (g_{ij})_p \geq 0.$$

The second step is the crucial one and it forms the basis of the results of this paper.

As regards the first step, the conductances of N_d can easily be obtained using Guillemin's approach [3] in terms of the entries of Y as outlined below.

Let Y_d be the cutset admittance matrix of the network of departure N_d of N obtained by augmenting Y with a row and column of zeros corresponding to the nonport

where the y_{ij} 's are the entries of the Y -matrix of N and the $(m+1)$ th row and column correspond to the nonport branch between the nodes $(m+1)$ and $(m+2)$ of T_0 . The edge conductances $(g_{ij})_d$'s of N_d are then as follows:

$$(g_{ij})_d = [(y_{i,j-1} + y_{i-1,j}) - (y_{i-1,j-1} + y_{ij})],$$

$$1 \leq i, j \leq m, i \neq j \quad (4a)$$

$$(g_{i,m+1})_d = (y_{i,m} - y_{i-1,m}), \quad 1 \leq i \leq m \quad (4b)$$

$$(g_{i,m+2})_d = (y_{i-1,m+1} - y_{i,m+1}), \quad 1 \leq i \leq m \quad (4c)$$

$$(g_{i,j})_d = [(y_{i,j-2} + y_{i-1,j-1}) - (y_{i-1,j-2} + y_{i,j-1})],$$

$$1 \leq i \leq m, (m+3) \leq j \leq (n+2) \quad (4d)$$

$$(g_{m+1,m+2})_d = y_{m,m+1} \quad (4e)$$

$$(g_{m+1,j})_d = (y_{m,j-1} - y_{m,j-2}), \quad (m+3) \leq j \leq (n+2) \quad (4f)$$

$$(g_{m+2,j})_d = (y_{m+1,j-2} - y_{m+1,j-1}), \quad (m+3) \leq j \leq (n+2) \quad (4g)$$

$$(g_{ij})_d = [(y_{i-1,j-2} + y_{i-2,j-1}) - (y_{i-2,j-2} + y_{i-1,j-1})],$$

$$(m+3) \leq i, j \leq (n+2), i \neq j. \quad (4h)$$

Before we state the theorem of this section, we need the following definitions. Let

$\bar{V}_1(\bar{V}_2)$ denote the subset of $V_1(V_2)$ such that for all $i \in \bar{V}_1(\bar{V}_2)$, $S_{i0} \neq 0$;

$x(y)$ denote the number of vertices in $\bar{V}_1(\bar{V}_2)$;

$D_1 = x \min \{(g_{ij})_d\}, i, j \in \bar{V}_1$;

$D_2 = y^2/x \min \{(g_{ij})_d\}, i, j \in \bar{V}_2$;

$D_3 = y \max \{|(g_{ij})_d|\}, i \in \bar{V}_1, j \in \bar{V}_2$ provided $(g_{ij})_d < 0$ and $L(D_1, D_2)$ denote the smaller of D_1 and D_2 .

Theorem 1

A real symmetric matrix Y of order n can be realized as the short-circuit conductance matrix of an $(n+2)$ -node resistive n -port network, containing no negative conductances and having a specified 2-tree port configuration

$$Y_d = \begin{array}{c} \left[\begin{array}{c} \uparrow \\ m \text{ rows} \\ \downarrow \\ (m+1) \text{ th} \\ \text{row} \\ \uparrow \\ (n-m) \\ \text{rows} \\ \downarrow \end{array} \right] \begin{array}{c} \left[\begin{array}{c} \leftarrow m \text{ columns} \rightarrow \\ \leftarrow (n-m) \\ \text{columns} \rightarrow \end{array} \right] \begin{array}{c} (m+1) \text{ th} \\ \text{column} \end{array} \end{array} \end{array}$$

$y_{1,1}$	\dots	$y_{1,m}$	0	$y_{1,m+1}$	\dots	$y_{1,n}$
\vdots	\dots	\vdots	\vdots	\vdots	\dots	\vdots
$y_{m,1}$	\dots	$y_{m,m}$	0	$y_{m,m+1}$	\dots	$y_{m,n}$
0	\dots	0	0	0	\dots	0
$y_{m+1,1}$	\dots	$y_{m+1,m}$	0	$y_{m+1,m+1}$	\dots	$y_{m+1,n}$
\vdots	\dots	\vdots	\vdots	\vdots	\dots	\vdots
$y_{n,1}$	\dots	$y_{n,m}$	0	$y_{n,m+1}$	\dots	$y_{n,n}$

tree branch of T_0 connecting T_1 and T_2

T , if

- i) for all $i, j \in V_1(V_2)$
 - a) $(g_{ij})_d \geq 0$
 - b) S_{i0} or S_{j0} or both are equal to zero if $(g_{ij})_d = 0$, and
- ii) $L(D_1, D_2) \geq D_3$.

Proof: We prove the theorem by establishing a procedure for the synthesis of the required n -port network N .

We note that conditions i)-a) and i)-b) of the theorem imply properties 1-3) and 3-1), respectively, of [6]. Let for the required network N

$$S_i = s_1 > 0, \quad i \in \bar{V}_1. \quad (5a)$$

$$S_j = s_2 > 0, \quad j \in \bar{V}_2. \quad (5b)$$

$$S_i = S_j = 0, \quad i, j \notin (\bar{V}_1 \cup \bar{V}_2). \quad (5c)$$

Then we have from (2) and (5)

$$S = xs_1 = ys_2. \quad (6)$$

Since N should contain no negative conductances, we have

$$|(g_{ij})_p| = \frac{S_i S_j}{S} \leq (g_{ij})_d, \quad i, j \in V_1(V_2), i \neq j. \quad (7)$$

For any $i, j \notin (\bar{V}_1 \cup \bar{V}_2)$ we have by (5c) that $S_i = S_j = 0$. Hence inequality (7) will always be satisfied if

$$i \notin \bar{V}_1(\bar{V}_2) \text{ or } j \notin \bar{V}_1(\bar{V}_2) \text{ or } i, j \notin \bar{V}_1(\bar{V}_2).$$

Further, in view of condition i)-b) of the Theorem 1, we get $(g_{ij})_d > 0$ for all $i, j \in \bar{V}_1(\bar{V}_2)$. Thus inequality (7) is equivalent to the following:

$$\frac{S_i S_j}{S} \leq (g_{ij})_d, \quad i, j \in \bar{V}_1(\bar{V}_2), i \neq j. \quad (8)$$

Using equations (5a) and (5b), we get from (8) the following:

$$\frac{s_1}{x} \leq (g_{ij})_d, \quad i, j \in \bar{V}_1 \quad \text{and} \quad \frac{xs_1}{y^2} \leq (g_{ij})_d, \quad i, j \in \bar{V}_2 \quad (9)$$

the latter following from the fact that $s_1 x = s_2 y$ (vide equation (6)).

Using the definitions of D_1, D_2 , and D_3 , we conclude from (9), that

$$s_1 \leq L(D_1, D_2). \quad (10)$$

Values of S_i 's obtained using (5) and value of S obtained in accordance with (10) will satisfy the inequality (7).

For N to contain no negative conductances, we also require that

$$(g_{ij})_p = \frac{S_i S_j}{S} \geq |(g_{ij})_d|, \quad i \in V_1, j \in V_2 \text{ provided } (g_{ij})_d < 0. \quad (11)$$

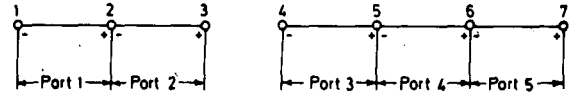


Fig. 2. Port configuration of network for Example 2.1.

We note that if $(g_{ij})_d < 0$, for any $i \in V_1$ and $j \in V_2$, then it follows from (3) that $S_{i0} \neq 0$ and $S_{j0} \neq 0$. Thus (11) is equivalent to the following:

$$\frac{S_i S_j}{S} \geq |(g_{ij})_d|, \quad i \in \bar{V}_1, j \in \bar{V}_2 \text{ provided } (g_{ij})_d < 0. \quad (12)$$

Using (5a), (5b), and (6) we then obtain from (12)

$$\frac{s_1}{y} \geq |(g_{ij})_d|, \quad i \in \bar{V}_1, j \in \bar{V}_2 \text{ provided } (g_{ij})_d < 0. \quad (13)$$

We then conclude from (13) that

$$s_1 \geq D_3. \quad (14)$$

Values of S_i 's obtained using (5) and any value of S obtained in accordance with (6) and (14) will satisfy inequality (11). Then from (10) and (14) we get that

$$D_3 \leq s_1 \leq L(D_1, D_2). \quad (15)$$

Since by condition ii) of the theorem $L(D_1, D_2) > D_3$, it is always possible to choose a value for s_1 lying in the range given by (15). Based on these discussions, we now state the following procedure to obtain the required network N realizing the matrix Y .

Step 1: Obtain the unique network of departure N_d with respect to the matrix Y and having the specified port configuration T .

Step 2: Choose s_1 so that $D_3 \leq s_1 \leq L(D_1, D_2)$.

Step 3: Obtain S_i 's using equations (5).

Step 4: Obtain the edge conductances of the padding network N_p using equations (1).

Step 5: The parallel combination of N_d and N_p realizes the given matrix Y .

Hence the theorem.

Example 2.1

Let it be required to realize the matrix

$$Y = \begin{bmatrix} 50 & 50 & -4 & 18 & 20 \\ 50 & 78 & -4 & 18 & 20 \\ -4 & -4 & 80 & 45 & 33 \\ 18 & 18 & 45 & 105 & 48 \\ 20 & 20 & 33 & 48 & 60 \end{bmatrix}$$

as the short-circuit conductance matrix of a resistive 5-port network having the port configuration shown in Fig. 2. We make use of the procedure given in Theorem 1. The conductances of the network of departure N_d with respect to Y and having the prescribed port configuration as

shown in Fig. 2 are (all in mhos) as follows:

$$G_d = \text{diag} \left\{ \begin{matrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{matrix} \right\}_d$$

$$= \text{diag} \left\{ \begin{matrix} 0 & 50 & 4 & -22 & -2 & 20 & 28 & 0 & 0 & 0 & 0 \\ -4 & 22 & 2 & -20 & 35 & 12 & 33 & 45 & 15 & 12 \end{matrix} \right\}.$$

We observe that conditions i)-a) and i)-b) of Theorem 1 are satisfied by N_d . We note that $x=2$ and $y=4$. We next obtain D_3 and $L(D_1, D_2)$ as follows:

$$D_1 = 50 \times 2 = 100, \quad D_2 = \frac{12 \times (4)^2}{2} = 96, \quad \text{and} \quad D_3 = 22 \times 4 = 88.$$

Since $96 = L(D_1, D_2) \geq D_3 = 88$, condition ii) of Theorem 1 is also satisfied.

We must choose a value of s_1 in the range $88 \leq s_1 \leq 96$. Choose $s_1 = 90$. Then, we get S_i 's using (5). They are as follows (all in mhos):

$$S_1 = 90, \quad S_2 = 0, \quad S_3 = 90, \quad S_4 = 45,$$

$$S_5 = 45, \quad S_6 = 45, \quad \text{and} \quad S_7 = 45.$$

Using (6), we get $S = 180$. The conductances of the required padding network having the above values of S_i 's are obtained using (1) and they are (all in mhos) as follows:

$$G_p = \text{diag} \left\{ \begin{matrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{matrix} \right\}_p$$

$$= \text{diag} \left\{ \begin{matrix} 0 & -45 & 22.5 & 22.5 & 22.5 & 22.5 & 0 & 0 & 0 & 0 & 0 \\ 22.5 & 22.5 & 22.5 & 22.5 & -\frac{45}{4} & -\frac{45}{4} & -\frac{45}{4} & -\frac{45}{4} & -\frac{45}{4} & -\frac{45}{4} & -\frac{45}{4} \end{matrix} \right\}.$$

The parallel combination N of N_d and N_p is a 5-port network realizing the given matrix Y . The conductances of N are given as (all in mhos):

$$G = \text{diag} \left\{ \begin{matrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{matrix} \right\}$$

$$= \text{diag} \left\{ \begin{matrix} 0 & 5 & 26.5 & 0.5 & 20.5 & 42.5 & 28 & 0 & 0 & 0 & 0 \\ 18.5 & 44.5 & 24.5 & 2.5 & 23.75 & 0.75 & 21.75 & 33.75 & 3.75 & 0.75 \end{matrix} \right\}.$$

III. $(n+2)$ -NODE REALIZABILITY OF UNIFORMLY TAPERED *Y*-MATRICES

In this section we establish that an $(n \times n)$ real symmetric uniformly tapered matrix Y can be realized as the short-circuit conductance matrix of an $(n+2)$ -node resistive n -port network N .

Let the ports and vertices of T_1 and T_2 be numbered as in Fig. 1.

The edge conductances of the network of departure N_d with respect to the matrix Y and the port configuration T (Fig. 1) can be obtained using (4).

Letting

$$s_i = \frac{S_i}{\sqrt{S}}$$

(1) of section 2 can be written as follows:

$$(g_{ij})_p = -s_i s_j, \quad i, j \in V_1(V_2), i \neq j \quad (16a)$$

$$(g_{ij})_p = s_i s_j, \quad i \in V_1(V_2), j \in V_2(V_1), i \neq j \quad (16b)$$

$$s = \sum_{i \in V_1} s_i = \sum_{j \in V_2} s_j. \quad (16c)$$

As mentioned in Section II, the crucial step in realizing the matrix Y is to make a suitable choice of nonnegative values for s_i 's so that the conductances $(g_{ij})_p$ obtained by

(16a) and (16b) will be such that $(g_{ij})_d + (g_{ij})_p \geq 0$ for all i and j , $i \neq j$.

Let us choose s_i 's so that the following are satisfied:

$$g_{ij} = (g_{ij})_d + (g_{ij})_p = 0, \quad i = 1, 2, 3, \dots, m \text{ and } j = (m+2), \quad (17)$$

and

$$g_{ij} = (g_{ij})_d + (g_{ij})_p = 0, \quad i = (m+1) \text{ and } j = (m+3), (m+4), \dots, (n+2). \quad (18)$$

On an examination of (4c), (4f), and (16b) it is clear that the conductances of N_d appearing in (17) and (18) are all negative and those of N_p nonnegative. Hence (17) and (18) may be rewritten as

$$g_{ij} = -|(g_{ij})_d| + (g_{ij})_p = 0, \quad i = 1, 2, 3, \dots, m \text{ and } j = (m+2)$$

$$g_{ij} = -|(g_{ij})_d| + (g_{ij})_p = 0, \quad i = (m+1) \text{ and } j = (m+3), (m+4), \dots, (n+2).$$

Using (4c), (4f), and (16b) in the above, we get

$$(y_{i-1,m+1} - y_{i,m+1}) + s_i s_{m+2} = 0, \quad i = 1, 2, 3, \dots, m$$

and

$$(y_{m,j-1} - y_{m,j-2}) + s_{m+1} s_j = 0, \quad j = (m+3), (m+4), \dots, (n+2).$$

On simplification of these, the following are obtained:

$$s_i = \frac{(y_{i,m+1} - y_{i-1,m+1})}{(s_{m+2})}, \quad i = 1, 2, 3, \dots, m \quad (19)$$

$$s_j = \frac{(y_{m,j-2} - y_{m,j-1})}{(s_{m+1})}, \quad j = (m+3), (m+4), \dots, (n+2). \quad (20)$$

It may be noted that the numerator and the denominator of the quantities appearing on the right-hand side of (19) and (20) are nonnegative because of the uniformly tapered property [1] of the given matrix Y .

In view of (17) and (18), we get

$$s_{m+1} = s_{m+2} = g_{m+1,m+2} / \sqrt{S}. \quad (21)$$

It may be verified that the values of s_i 's obtained using (19), (20), and (21) satisfy the relation (16c), i.e.,

$$s = \sum_{i \in V_1} s_i = \sum_{j \in V_2} s_j.$$

It remains to check whether the above choice for s_i 's results in nonnegative values for all the edge conductances of N . The conductances (other than those set to zero in (17) and (18)) that have to be tested for nonnegativeness can be classified into three groups as follows.

Group I: a) $g_{ij}, i = 1, 2, 3, \dots, m$ and $j = (m+3), (m+4), \dots, (n+2)$.

b) $g_{m+1,m+2}$.

Group II: a) $g_{ij}, i = 1, 2, 3, \dots, m$ and $j = (m+1)$.

b) $g_{ij}, i = (m+2); j = (m+3), (m+4), \dots, (n+2)$.

Group III: a) $g_{ij}, i, j = 1, 2, 3, \dots, m, i \neq j$.

b) $g_{ij}, i, j = (m+3), (m+4), \dots, (n+2), i \neq j$.

The conductances of Group I can be shown to be nonnegative using (4d), (4e), and (16b) and the uniformly tapered property [1] of Y .

The conductances of Group II can be expressed using (4b), (4g), (16a), (19), (20), and (21) as

$$g_{i,m+1} = [(y_{i,m} + y_{i-1,m+1}) - (y_{i-1,m} + y_{i,m+1})], \quad i = 1, 2, 3, \dots, m \quad (22)$$

$$g_{m+2,j} = [(y_{m+1,j-2} + y_{m,j-1}) - (y_{m,j-2} + y_{m+1,j-1})], \quad j = (m+3), (m+4), \dots, (n+2). \quad (23)$$

The right-hand side of the above equations are nonnegative because of the uniformly tapered property [1] of Y . Hence the conductances of Group II are also nonnegative.

The nonnegativeness of the conductances of Group III yields the following inequalities:

$$g_{ij} = (g_{ij})_d + (g_{ij})_p \geq 0, \quad i, j = 1, 2, 3, \dots, m, i \neq j \quad (24)$$

$$g_{ij} = (g_{ij})_d + (g_{ij})_p \geq 0,$$

$$i, j = (m+3), (m+4), \dots, (n+2), i \neq j. \quad (25)$$

Using (4a), (19), and (21) in (24) we obtain the following:

$$(s_{m+1})^2 \geq \left[\frac{(y_{i,m+1} - y_{i-1,m+1})(y_{j,m+1} - y_{j-1,m+1})}{(y_{i,j-1} + y_{i-1,j}) - (y_{i-1,j-1} + y_{ij})} \right] = C_{ij}, \quad i, j = 1, 2, 3, \dots, m, i \neq j. \quad (26)$$

Similarly using (4h), (20), and (21) in inequality (25), we get

$$(s_{m+1})^2 \geq \left[\frac{(y_{m,i-2} - y_{m,i-1})(y_{m,j-2} - y_{m,j-1})}{(y_{i-1,j-2} + y_{i-2,j-1}) - (y_{i-2,j-2} + y_{i-1,j-1})} \right] = D_{ij}, \quad i, j = (m+3), (m+4), \dots, (n+2), i \neq j. \quad (27)$$

It may be noted that the numerator and the denominator of the right-hand side of the inequalities (26) and (27) are nonnegative because of the uniformly tapered property of Y .

Letting

$$C = \max \{ C_{ij} \}, \quad i, j = 1, 2, 3, \dots, m, i \neq j$$

$$D = \max \{ D_{ij} \}, \quad i, j = (m+3), (m+4), \dots, (n+2), i \neq j$$

we get from (26) and (27)

$$(s_{m+1})^2 \geq \max \{ C, D \}. \quad (28)$$

Once a choice of $(s_{m+1})^2$ is made using (28), all other s_i 's can be obtained using (19), (20), and (21). Such a choice of s_i 's will result in nonnegative values for the conductances of the required network N .

It can be seen that there will be in general, $n(n+1)+2/2$ nonzero conductances in N . When $(s_{m+1})^2$ is chosen to be equal to $\max \{ C, D \}$, then, N will contain $n(n+1)/2$ conductances.

Further when $(s_{m+1})^2$ tends to infinity, all other s_i 's will tend to zero and $g_{m+1,m+2}$ will tend to infinity. Thus the

nodes $(m + 1)$ and $(m + 2)$ will merge into one and the network N will be the same as the $(n + 1)$ -node realization of Y .

It may be noted that if any one $(g_{ij})_d = 0$, for $i, j = 1, 2, 3, \dots, m, i \neq j$ or $i, j = (m + 3), (m + 4, \dots, (n + 2), i \neq j$, then the denominator of (26) or (27) will be zero. Hence $(s_{m+1})^2$ tends to infinity in which case the resulting realization is only an $(n + 1)$ -node n -port. In this situation if one is interested only in an $(n + 2)$ -node n -port realization, one can always choose m such that there is no zero edge conductance connecting two vertices in the same connected part T_1 or T_2 of the port configuration T of the network of departure N_d . If, for a chosen m , there happens to be more number of zero edge conductances on the vertices of T_1 or T_2 of the port configuration T of the network of departure N_d , a suitable value for m can be selected such that the realization results in an $(n + 2)$ -node n -port, provided all such edges of zero conductances form part of a single cut-set, with respect to the port tree of the $(n + 1)$ -node realization.

Thus we have the following theorem on resistive n -port realizability of Y -matrices on two-tree port structures:

Theorem 2

i) An $(n \times n)$ real symmetric uniformly tapered matrix can be realized as the short-circuit conductance matrix of

$$G_d = \text{diag} \begin{Bmatrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ & g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{Bmatrix}_d$$

$$= \text{diag} \begin{Bmatrix} 16 & 8 & 24 & -16 & 8 & 8 & 16 & 12 & -8 & 4 & 4 \\ & 20 & -4 & 2 & 2 & 28 & -14 & -14 & 30 & 16 & 16 \end{Bmatrix}.$$

an $(n + 2)$ -node resistive n -port network N containing at most $n(n + 1)/2$ conductances, provided its $(n + 1)$ -node n -port realization contains no zero conductances.

ii) If the $(n + 1)$ -node realization N of the given matrix contains some zero conductances, then also an $(n + 2)$ -node realization containing at most $n(n + 1)/2$ conductances is possible provided all such zero conductances form part of a single fundamental cut-set with respect to the port tree of N .

The above theorem leads to the following Corollary which can easily be proved.

Corollary 1

i) An $(n \times n)$ real symmetric matrix realizable by an $(n + 1)$ -node resistive n -port network N_1 containing no zero conductances can be realized by an $(n + 2)$ -node n -port network N_2 containing at most $n(n + 1)/2$ conductances.

ii) If the $(n + 1)$ -node realization N_1 contains some zero conductances, then an equivalent $(n + 2)$ -node realization N_2 containing at most $n(n + 1)/2$ conductances is possible, provided all such zero conductances form part of a

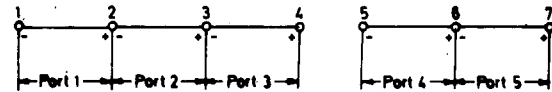


Fig. 3. Port configuration of network for Example 3.1.

single fundamental cut-set with respect to the port tree of N_1 .

Example 3.1

Let it be required to realize the uniformly tapered matrix

$$Y = \begin{bmatrix} 48 & 32 & 24 & 16 & 8 \\ 32 & 60 & 36 & 24 & 12 \\ 24 & 36 & 56 & 28 & 14 \\ 16 & 24 & 28 & 46 & 16 \\ 8 & 12 & 14 & 16 & 32 \end{bmatrix}$$

as the short-circuit conductance matrix of a resistive 5-port network having the port configuration shown in Fig. 3.

We see that $m = 3$ for the port configuration given in Fig. 3. Using (4), we calculate the edge conductances in the network of departure with respect to Y and the prescribed port configuration given in Fig. 3. They are (all in mhos) as follows:

In accordance with (17) and (18), we make the following edge conductances in the final network N to be equal to zero, i.e.,

$$g_{15} = g_{25} = g_{35} = g_{46} = g_{47} = 0.$$

The edge conductances that belong to Group III are

$$g_{12}, g_{13}, g_{23}, \text{ and } g_{67}.$$

The condition that these edge conductances are to be nonnegative yields from (26) and (27), respectively, the following:

$$s_4^2 \geq 8, \quad s_4^2 \geq 8, \quad s_4^2 \geq 2, \quad \text{and} \quad s_4^2 \geq \frac{49}{4}.$$

It is seen that

$$C = \max\{8, 8, 2\} \quad \text{and} \quad D = \max\left\{\frac{49}{4}\right\}$$

and therefore, $s_4^2 \geq \max\{(C, D)\} = 49/4$. Let us choose $s_4^2 = 16$, which gives $s_4 = 4$. We now make use of (19), (20), and (21) and calculate the values of all the s_i 's. They are

as follows:

$$s_1 = 4, \quad s_2 = 2, \quad s_3 = 1, \quad s_4 = s_5 = 4, \\ s_6 = \frac{7}{2}, \quad \text{and} \quad s_7 = \frac{7}{2}.$$

The conductances of the required padding network having the above values of s_i 's are obtained using (16) as

$$G_p = \text{diag} \begin{Bmatrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{Bmatrix}_p \\ = \text{diag} \begin{Bmatrix} -8 & -4 & -16 & 16 & 14 & 14 & -2 & -8 & 8 & 7 & 7 \\ -4 & 4 & 3.5 & 3.5 & 16 & 14 & 14 & -14 & -14 & -12.25 \end{Bmatrix}.$$

The parallel combination N of N_d and N_p is a 5-port network realizing the given uniformly tapered matrix Y . The conductances of N are given (all in mhos) as follows:

$$G = \text{diag} \begin{Bmatrix} g_{12} & g_{13} & g_{14} & g_{15} & g_{16} & g_{17} & g_{23} & g_{24} & g_{25} & g_{26} & g_{27} \\ g_{34} & g_{35} & g_{36} & g_{37} & g_{45} & g_{46} & g_{47} & g_{56} & g_{57} & g_{67} \end{Bmatrix} \\ = \text{diag} \begin{Bmatrix} 8 & 4 & 8 & 0 & 22 & 22 & 14 & 4 & 0 & 11 & 11 \\ 16 & 0 & 5.5 & 5.5 & 44 & 0 & 0 & 16 & 2 & 3.75 \end{Bmatrix}.$$

IV. CONCLUSIONS

In this paper, realizability of an $(n \times n)$ real symmetric matrix as the short-circuit conductance matrix of an $(n+2)$ -node resistive n -port network is investigated. Two sufficient conditions are established in Sections II and III. Guillemin's approach [3] and the formulas developed in [6] for the conductances of an $(n+2)$ -node padding n -port network are used in arriving at the results.

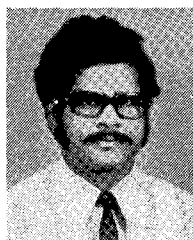
The $(n+2)$ -node realizability of uniformly tapered Y -matrices, established in Section III leads to Corollary 1, namely, that any Y -matrix realizable by an $(n+1)$ -node n -port network containing $n(n+1)/2$ conductances, can be realized by an $(n+2)$ -node network containing $n(n+1)/2$ conductances. This result means that if an $(n+2)$ -node n -port network N_1 has more than $n(n+1)/2$ conductances, and if its Y -matrix is also realizable by an $(n+1)$ -node network containing $n(n+1)/2$ conductances, then an equivalent network N_2 , containing $n(n+1)/2$ conductances can be obtained.

REFERENCES

- [1] E. A. Guillemin, "On the analysis and synthesis of single-element-kind n -port networks," *I.R.E. Trans. Circuit Theory*, vol. CT-7, pp. 303-312, Sept. 1960.
- [2] F. T. Boesch and D. C. Youla, "Synthesis of $(n+1)$ -node resistor n -ports," *IEEE Trans. Circuit Theory*, vol. CT-12, pp. 515-520, Dec. 1965.
- [3] E. A. Guillemin, "On the realization of an n th-order G -matrix," *IEEE Trans. Circuit Theory*, vol. CT-8, pp. 318-323, Sept. 1961.
- [4] P. S. Reddy, V. G. K. Murti, and K. Thulasiraman, "Realization of modified cut-set matrix and applications," *IEEE Trans. Circuit Theory*, vol. CT-17, pp. 475-486, Nov. 1970.

- [5] K. R. Swaminathan and I. T. Frisch, "Necessary conditions for the realizability of n -port resistive networks with more than $(n+1)$ nodes," *IEEE Trans. Circuit Theory*, vol. CT-12, pp. 520-527, Dec. 1965.
- [6] P. S. Reddy and K. Thulasiraman, "Synthesis of $(n+2)$ -node resistive n -port networks," *IEEE Trans. Circuit Theory*, vol. CT-19, pp. 20-25, Jan. 1972.
- [7] C. G. Jambotkar and Y. Tokad, "Realization of n th-order matrices with two-tree port structures," *Journal of the Franklin Institute*, vol. 288, no. 4, pp. 245-260, Oct. 1969.

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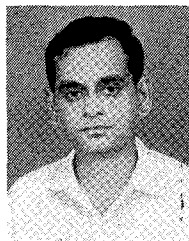
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L_∞ - and l_∞ -Stability of Interconnected Systems

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Abstract—Sufficient conditions for the L_∞ - and l_∞ -boundedness of nonlinear interconnected systems are established. Systems which may be viewed as an interconnection of single-loop feedback systems are considered. Overall boundedness conditions are phrased in terms of the margins by which each subsystem satisfies a certain boundedness condition. The existence of similar results for the L_∞ - and l_∞ -continuity of nonlinear interconnected systems is noted.

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I. INTRODUCTION

NEW RESULTS FOR L_∞ - and l_∞ -stability of a large class of interconnected feedback systems (also called composite or large-scale systems) are established. Specifically, systems are considered which may be viewed as an interconnection of single-loop feedback systems (with single inputs and single outputs). Each such single loop, regarded as an input-output system in its own right, shall be termed an "isolated subsystem," while the remaining system elements comprise the "interconnecting structure." In the present approach, the objective is to analyze composite systems in terms of their lower order and simpler subsystems and in terms of their interconnecting structure.