Performance of Output-Multibuffered Multistage Interconnection Networks Under Non-Uniform Traffic Patterns

Bin Zhou

Department of Computer Science and Computer Engineering La Trobe University Melbourne 3083, Australia binz@latcs1.lat.oz.au

Abstract

The objective of this paper is to develop an analytical model to evaluate the throughput and packet delay, in the presence of nonuniform traffic, in a MIN having multiplebuffers at the output of the switching elements. The model is based on Markov chains, and uses several simplifying assumptions to make the model tractable. The validity of the model has been verified by comparison of the results with those obtained from simulations.

1 Introduction

It is known that the maximum achievable throughput for large sized input buffered-MINs with a single-buffer is limited to approximately 0.45 under uniform input traffic pattern. Even with infinite-sized input buffers, the maximum throughput of a large multi-buffered MIN is limited to approximately 0.75. Output buffered Banyan structure have previously been considered in the literature. Kim [1] reported a queueing analysis and a simulation study of output-buffered Banyans with an arbitrary (finite) buffer size. Atiquzzaman [2] proposed an efficient Markov chain model for performance evaluation of a single buffered Omega network in the presence of a hot spot. The aim of this paper is to develop a generalized analytical model for performance evaluation of output-multibuffered MINs under nonuniform and uniform traffic environments, particularly in the presence of a hot spot traffic.

2 Modeling Assumptions

An Omega network connects N processors to N memories using $n = \log_2 N$ stages of N/2 SEs per stage. Each output link of a SE has a finite number of buffers. The buffered Omega network has input buffer controllers (IBCs) added to each input of the network.

We assume a synchronous network. A backpressure mechanism ensures that no packets are lost within the network. The arrival process at each input of the network is a simple Bernoulli process. Each input link of the network is offered the same traffic load. There is no blocking at the output links of the network. The conflict resolution logic at each SE is fair.

Figure 1 shows three consecutive SEs in successive stages of the network. The input and output ports of

M. Atiquzzaman

Department of Computer Science and Computer Engineering La Trobe University Melbourne 3083, Australia atiq@latcs1.lat.oz.au



Figure 1: Modeling of single queue.

the l-th SE at stage k are denoted by klx, $kl\underline{x}$, kly and kly.

A buffer in a SE is modeled as a Markov chain. The state of a buffer is represented by the number of packets in the buffer. We first model a single queue, then link up the single queues into a network. The equations describing the dynamics of the network are described by recurrence relations. An iterative procedure [2] is used to solve the Markov chain. The procedure is based on decomposing the buffers in the stages and solving the stages successively. The probability of departure from a buffer is determined by the possibility of conflict with a packet at the same stage and the availability of buffer space at the SE of the next stage. We assume that a buffer supports simultaneous enqueueing and dequeueing of packets during a cycle. The performance measures are then obtained by using the steady state parameters of the system. We define h as the hot spot probability.

3 Results and Comparisons

The analytical model can be applied to any non-uniform traffic pattern since the model assumes an arbitrary general traffic pattern. Figure 2 shows a comparison of the normalized throughput obtained from the analytical model and simulation for uniform and nonuniform traffic patterns for an 8×8 Omega network with buffer size (m)=16. The low accuracy at a very high offered network traffic load for uniform traffic pattern results from several independence assumptions that have been made in the analysis. It was assumed in the model that packets arrive at the buffers independent of each other, and $P_{klxy}=0.5$ at all instants of time. In reality, blocked packets remain in their buffers in the preceding stage and contend for the same output, and hence P_{klxy} should be one in the next clock cycle, i.e., there is correlation between con-

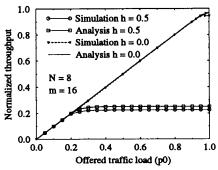


Figure 2: Throughput versus offered traffic load.

secutive clock cycles. Moreover there is correlation between the states of the buffers in adjacent stages. For h = 0.5, and low network traffic load, the analytical results are the same as simulation results. In Figure 3, we plot the normalized throughput for an offered traffic load (p_0) of 1.0. As the hot spot probability increases, the normalized throughput of the network decreases. When h = 0 (i.e., uniform traffic pattern), the maximum throughput of 0.96 is achieved. When hequals 1, (i.e., all processors are making hot requests.) the normalized throughput decreases to 1/N. As h increases from 0 to 0.4, there is a significant drop in the throughput. This degradation of the perfor-mance is caused by tree saturation. Figure 4 shows the comparison of analytical and simulation results for mean transfer time versus normalized throughput for an 8×8 network with m = 16 and $p_0 = 1.0$. h is varied from 0 to 1.0 to obtain the different throughputs. It shows how the hot requests affect the network delay and throughput. When h = 1, the network has the minimum throughput of 1/N and infinite delay. When h decreases, the throughput increases and the delay decreases. When h=0, a maximum throughput of 0.95 and minimum delay of 38 clock cycles is obtained. Figure 5 plots the mean transfer time (clocks) of an 8×8 network with m = 16 versus offered traffic load. It shows that considerable network congestion occurs at $p_0 = 0.9$ when h = 0. A tree saturation occurs at $p_0 = 0.25$ when h = 0.5.

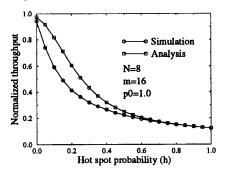


Figure 3: Throughput versus hot spot probability.

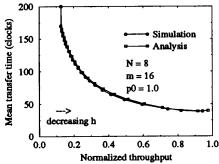


Figure 4: Mean transfer time versus throughput.

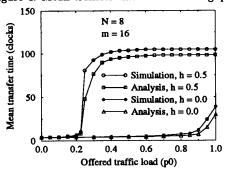


Figure 5: Packet delay.

4 Conclusion

An analytical model based on the Markov chain has been developed to evaluate the performance of output-multibuffered Omega network under nonuniform traffic environment. It can be applied to both uniform and nonuniform traffic patterns. The model is general enough to handle networks with arbitrary buffer sizes and switch sizes. It can be applicable to other types of networks as well, such as the Banyan and Baseline networks. Simulation and analytical results have been found to be in close agreement. The low accuracy at high loads results from several independence assumptions that have been made in the model. Development of an analytical model for output multibuffered multistage interconnection networks by considering the correlations between consecutive clock cycles as well as the states of the buffers in the adjacent stages will be reported.

References

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